



1990 Applications Handbook

**A/D Converters
D/A Converters
Analog Switches
Analog Multiplexers
Active Filters
Power Supply Circuits**

**Video Products
RS-232/Interface Circuits
Op Amps/Buffers
Voltage References
Display Drivers
Timers/Counters**

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POWER SUPPLY & DC-DC CONVERTERS

LINEAR REGULATORS

POSITIVE LOW POWER

- ICL7663 (variable)
- MAX663 (+5V or variable)
- MAX666 (+5V or var. inc. low batt. output)
- MAX667 (low dropout, +5V or variable)

NEGATIVE LOW POWER

- ICL7664
- MAX664 (-5V or variable)

SWITCHING REGULATORS

STEP UP

- MAX4193 (variable)
- MAX630 (variable)
- MAX631 (+5V or variable)
- MAX632 (+12V or variable)
- MAX633 (+15V or variable)
- MAX654 (+5Vout, +1Vin)
- MAX655 (+5Vout, +2Vin)
- MAX656 (+5Vout, +1Vin, Ext. FET)
- MAX657 (+3Vout, +1Vin)
- MAX658 (+5Vout, +2Vin, Ext. FET)
- MAX659 (+3Vout, +2Vin)

INVERTING

- MAX4391 (variable)
- MAX634 (variable)
- MAX635 (-5V or variable)
- MAX636 (-12V or variable)
- MAX637 (-15V or variable)

STEP DOWN

- MAX638 (+5V or variable)

DUAL OUTPUT

- MAX743 ($\pm 15V$ or $\pm 12V$)

EXT. FET TO APPROX. 5 WATTS STEP UP/STEP DOWN/INV.

- MAX641 (+5V or variable)
- MAX642 (+12V or variable)
- MAX643 (+15V or variable)

CHARGE PUMPS

-Vin and 2x Vin

- ICL7660
- ICL7662 (high voltage)
- Si7661 (high voltage)

2x Vin AND -2x Vin

- MAX680
- MAX681 (caps incl.)

μP SUPERVISORY CIRCUITS

FIVE FUNCTION* 16 PIN

- MAX691 (4.65V reset)
- MAX693 (4.0V reset)
- MAX695 (200ms reset pulse width)
- MAX791 (monitor backup batt)

FOUR FUNCTION* 16 PIN

- MAX696 (adj. reset threshold)
- MAX697 (adj. reset threshold)

FOUR FUNCTION* 8 PIN

- MAX690 (4.65 reset)
- MAX692 (4.0V reset)
- MAX694 (200ms reset pulse width)
- MAX790 (improved MAX690)

RESET & WATCHDOG

- MAX698 (reset only)
- MAX699
- MAX700 (reset only, adj hyst)
- MAX701 (reset only)
- MAX702 (reset only)
- MAX1232 (improved DS1232)

UNDER/OVER VOLTAGE DETECTORS

SINGLE VOLTAGE DETECTORS

- MAX8211 (non-inverting)
- MAX8212 (inverting)

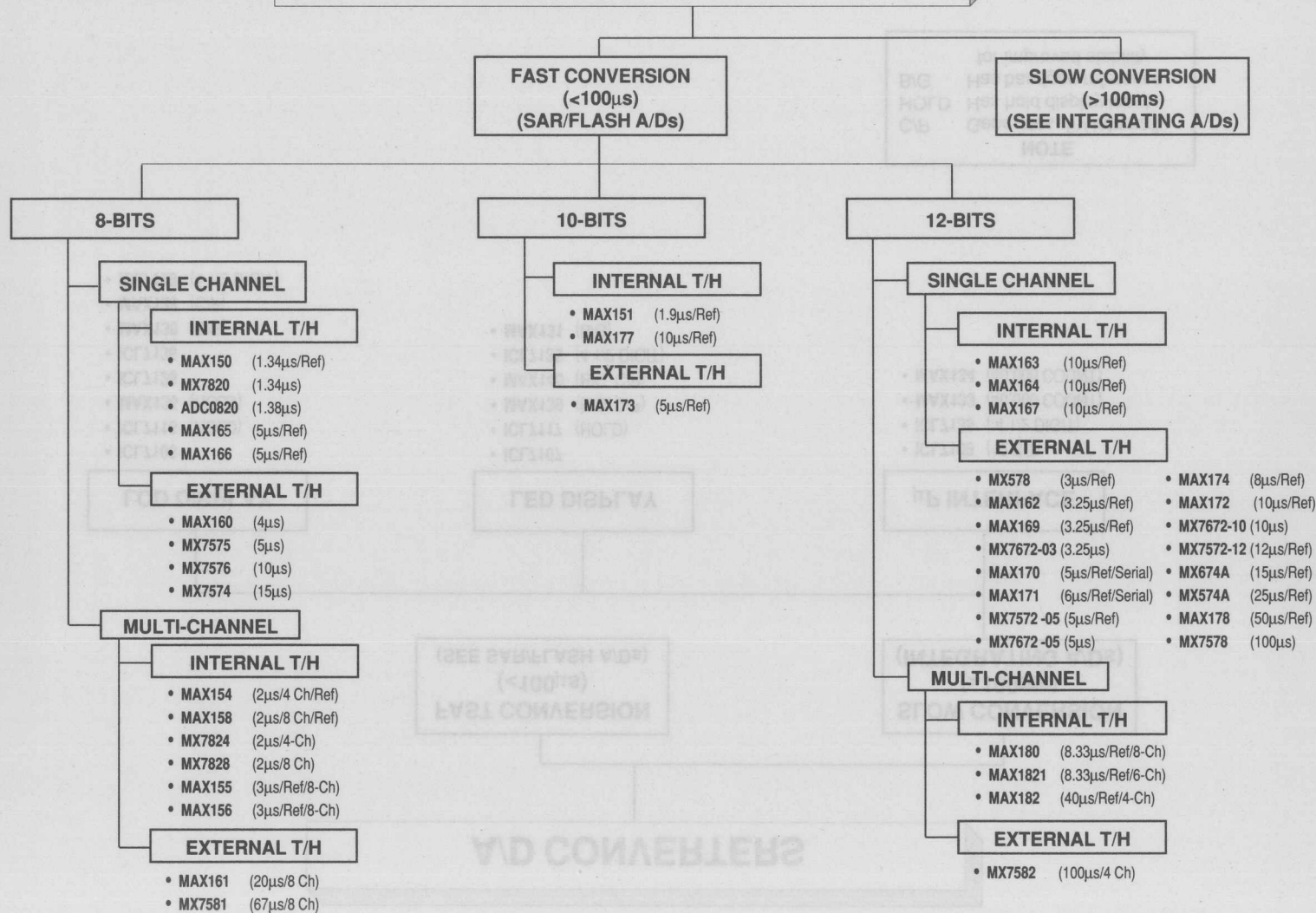
DUAL VOLTAGE DETECTORS

- ICL7665

* FUNCTION TABLE:

MAX690-MAX1232 FUNCTIONS	690	691	692	693	694	695	696	697	698	699	700	701	702	790	791	MAX 1232
Fixed Power Up/ Down Reset	✓	✓	✓	✓	✓	✓			✓	✓	✓	4	✓	✓	✓	✓
Variable Power Up/ Down Reset							✓	✓			✓					4
Battery Backup Switching	✓	✓	✓	✓	✓	✓	✓							✓	4	
Watchdog Timer	✓	✓	✓	✓	✓	✓	✓	✓		✓				✓	4	✓
Power Fail Warning	✓	✓	✓	✓	✓	✓	✓	✓						✓	4	
Write Protect		✓		✓		✓		✓							✓	

A/D CONVERTERS



A/D CONVERTERS

FAST CONVERSION
($<100\mu\text{s}$)
(SEE SAR/FLASH A/Ds)

SLOW CONVERSION
($>100\text{ms}$)
(INTEGRATING A/Ds)

LCD DISPLAY

- ICL7106
- ICL7116 (HOLD)
- MAX136 (HOLD)
- ICL7126
- ICL7136
- MAX130 (B/G)
- MAX138 (C/P)
- ICL7129 (4 1/2 DIGIT)

LED DISPLAY

- ICL7107
- ICL7117 (HOLD)
- MAX139 (B/G, C/P)
- MAX140 (B/G, C/P)
- ICL7135 (4 1/2 DIGIT)
- MAX131 (B/G)

μP INTERFACE

- ICL7109 (12 BIT)
- ICL7135 (4 1/2 DIGIT)
- MAX133 (40,000 COUNT)
- MAX134 (40,000 COUNT)

NOTE

C/P Generates -5V internally
HOLD Has hold display input
B/G Has bandgap reference for improved stability

DACs

RESOLUTION

8 BIT

V OUT

- MX7224
- MX7225 (Quad)
- MX7226 (Quad)
- MX7228 (Octal)
- MAX500 (Quad, Serial)

I OUT

- MX7523
- MX7524
- MX7528 (Dual)
- MX7628 (Dual)
- MAX7624

10 BIT

I OUT

- MX7520
- MX7530
- MX7533

12 BIT

V OUT

- MX7245 (Ref)
- MX7248 (Ref)
- MX7845 (MDAC)
- MAX501 (MDAC)

I OUT

- MX565A (Ref)
- MX566A
- MX7521
- MX7531
- MX7541
- MX7541A
- MX7542
- MX7543 (Serial)
- MX7545
- MX7545A
- MAX543 (Serial)
- MX7537 (Dual)
- MX7547 (Dual)

14 BIT

I OUT

- MX7534
- MX7535
- MX7536
- MX7538

REFERENCES

REFERENCES

REFERENCES

VOLTAGE OUT

1.2 Volts

- ICL8069
(10-100ppm/°C)

2.5 Volts

- MX580
(10-85ppm/°C)
- MX584
(10-30ppm/°C)

5.0 Volts

- MAX675
(12-20ppm/°C)
- REF02
(8.5-250ppm/°C)
- MX584
(5-30ppm/°C)

7.5 Volts

- MX584
(5-30ppm/°C)

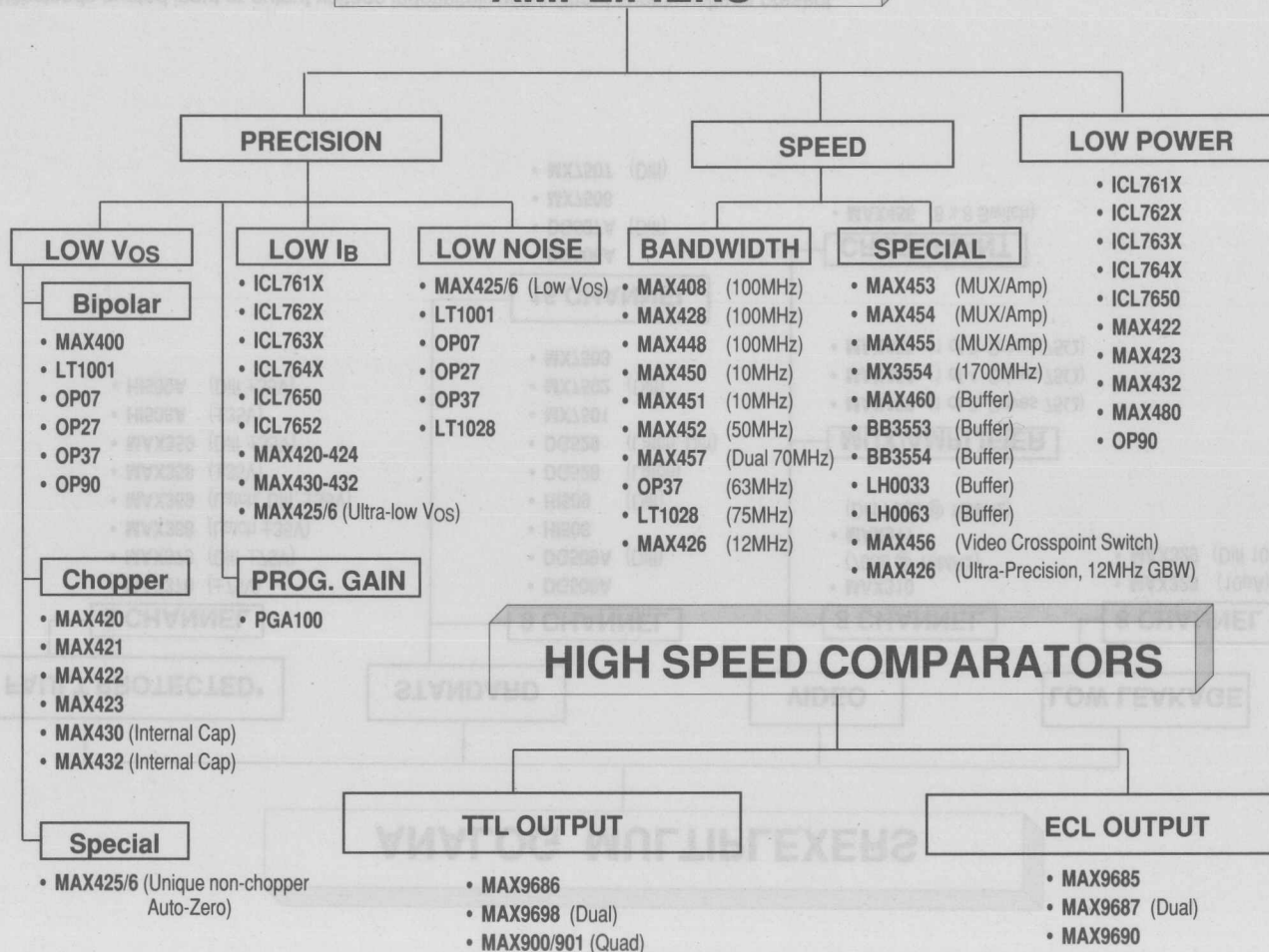
10.0 Volts

- MAX670
(3-10ppm/°C)
- MAX671
(1-10ppm/°C)
- MAX674
(12-20ppm/°C)
- MX2700
(3-10ppm/°C)
- MX2710
(1-5ppm/°C)
- MX581
(5-30ppm/°C)
- MX584
(5-30ppm/°C)
- REF01
(8.5-65ppm/°C)

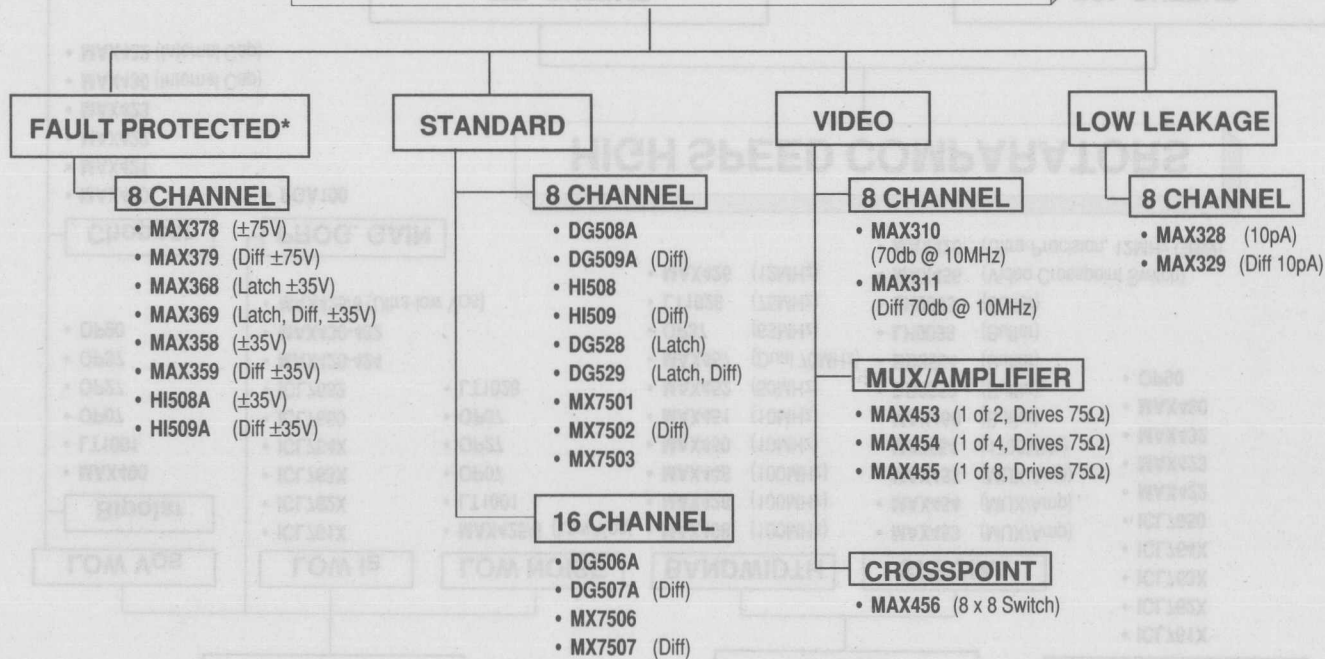
-10.0 Volts

- MX2701
(3-10ppm/°C)

AMPLIFIERS

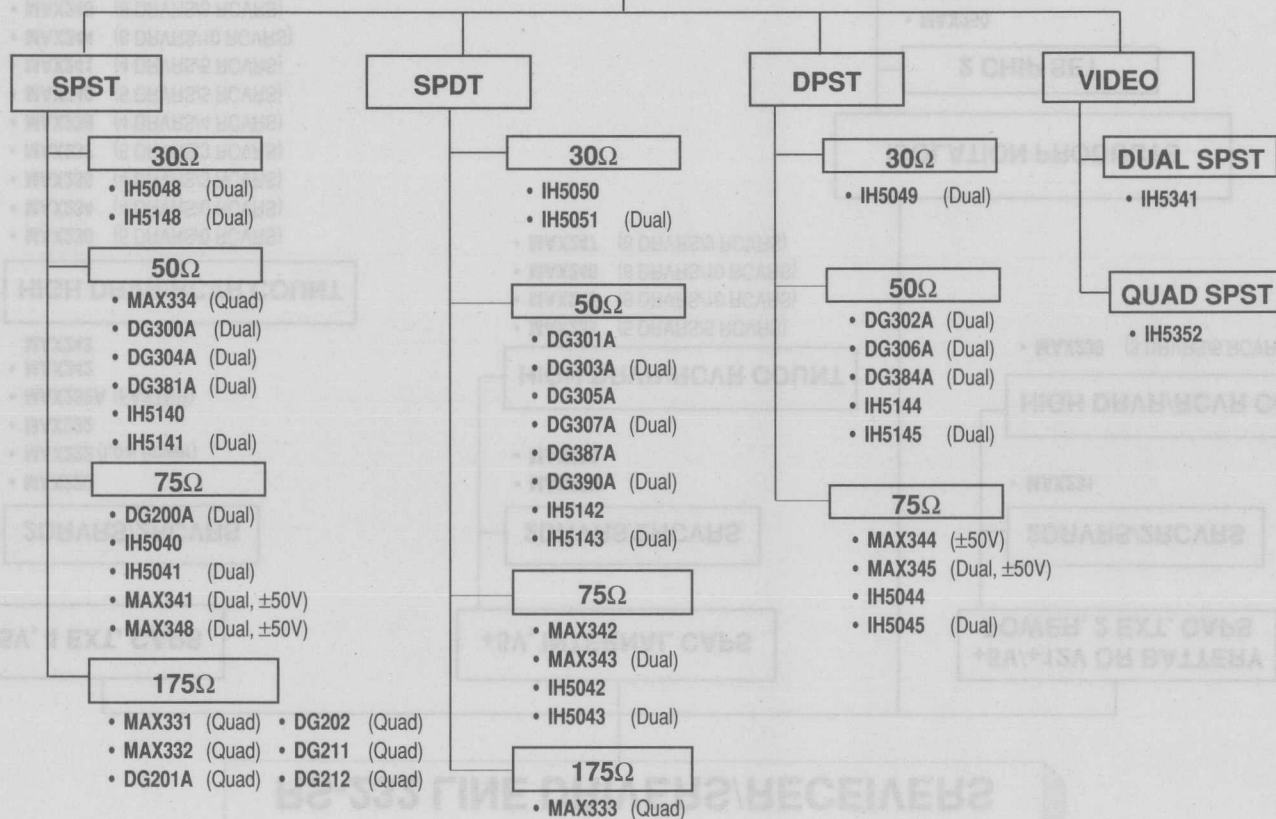


ANALOG MULTIPLEXERS



* Withstands quoted input or output voltage indefinitely with/without supply voltage present.

ANALOG SWITCHES



RS-232 LINE DRIVERS/RECEIVERS

+5V, 4 EXT. CAPS

2DRVRS/2RCVRS

- MAX220
- MAX222 (Low Power)
- MAX232
- MAX232A (FASTER)
- MAX242
- MAX243

HIGH DRVRS/RCVR COUNT

- MAX230 (5 DRVRS/0 RCVRS)
- MAX234 (4 DRVRS/0 RCVRS)
- MAX236 (4 DRVRS/3 RCVRS)
- MAX237 (5 DRVRS/3 RCVRS)
- MAX238 (4 DRVRS/4 RCVRS)
- MAX240 (5 DRVRS/5 RCVRS)
- MAX241 (4 DRVRS/5 RCVRS)
- MAX244 (8 DRVRS/10 RCVRS)
- MAX248 (8 DRVRS/8 RCVRS)
- MAX249 (6 DRVRS/10 RCVRS)

+5V, INTERNAL CAPS

2DRVRS/2RCVRS

- MAX223
- MAX233

HIGH DRVRS/RCVR COUNT

- MAX235 (5 DRVRS/5 RCVRS)
- MAX245 (8 DRVRS/10 RCVRS)
- MAX246 (8 DRVRS/10 RCVRS)
- MAX247 (8 DRVRS/9 RCVRS)

+5V/+12V OR BATTERY POWER, 2 EXT. CAPS

2DRVRS/2RCVRS

- MAX231

HIGH DRVRS/RCVR COUNT

- MAX239 (3 DRVRS/5 RCVRS)

ISOLATION PRODUCTS

2 CHIP SET

- MAX250
- MAX251

COMPLETE MODULE

- MAX252

ACTIVE FILTERS

SWITCHED CAPACITOR FILTERS

CONTINUOUS FILTERS

UNIVERSAL

μP PROG.

- MAX260 (7.5kHz)
- MAX261 (57kHz)
- MAX262 (140kHz)

PIN PROG.

- MAX263 (57kHz)
- MAX264 (140kHz)

RESISTOR PROG

- MAX265 (57kHz)
- MAX266 (140kHz)

BANDPASS PIN PROG.

- MAX 267 (57kHz)
- MAX268 (140kHz)

ZERO ERROR LOWPASS

- MAX280 (20kHz)
- LTC1062 (20kHz)
- MAX281 (20kHz)

LOWPASS, 2nd ORDER

- MAX270 (1-25kHz)
- MAX271 (1-25KHz)

DC-DC Converter and Switching Regulator Circuits

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DC-DC Converter and Switching Regulator Circuits

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The table lists measured efficiency for the indicated coils. Efficiencies can be improved slightly by placing a Schottky diode such as the 1N5817 in parallel with the internal MAX631/632/633 diode, from pin 4 to 5. The increase in efficiency is most noticeable for the 5V output circuits.

Maxim Part No.	V _{IN} (V)	V _{OUT} (V)	I _{OUT} (mA)	Typ Eff (%)	Inductor (L)		
					Part No.*	μH	Ω
MAX631	2	5	5	78	6860-21	470	0.44
	2	5	10	74	6860-17	220	0.28
	2	5	15	61	6860-13	100	0.1
	3	5	25	82	6860-21	470	0.44
	3	5	40	75	7070-21	220	0.55
MAX632	3	12	5	79	6860-10	330	0.35
	3	12	10	79	7070-28	180	0.48
	5	12	12	88	6860-21	470	0.44
	5	12	25	87	6860-19	330	0.35
MAX633	3	15	5	73	7070-29	220	0.55
	3	15	8	71	7070-27	150	0.43
	5	15	10	85	6860-21	470	0.44
	5	15	15	85	6860-19	330	0.35
	8	15	35	90	6860-21	470	0.44

*Caddell-Burns, NY, (516) 746-2310

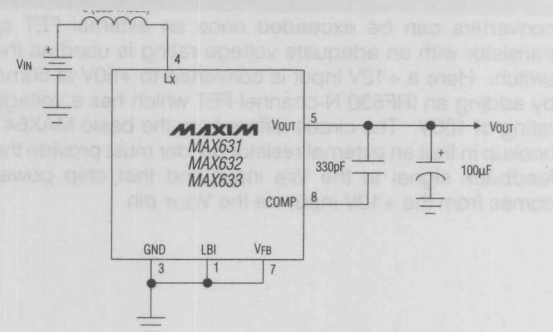


Figure 1-1.

Medium Power Step-Up Converters

In selecting coils for DC-DC converter circuits that use external MOSFETs it is important to calculate the peak current and to select a coil that will not saturate at that peak current.

Maxim Part No.	V _{IN} (V)	V _{OUT} (V)	I _{OUT} (mA)	Typ Eff (%)	I _{PK} (A)	Inductor (L)		
						Part No.*	μH	Ω
MAX642	5	12	200	91	1.2	6860-08	39	0.05
	5	12	350	89	2	6860-04	18	0.03
	5	12	550	87	3.5	7200-02	12	0.01
MAX643	5	15	100	92	1.2	6860-08	39	0.05
	5	15	150	89	1.5	6860-06	27	0.04
	5	15	225	89	2	6860-04	18	0.03
	5	15	325	85	3.5	7200-02	12	0.01

*Caddell-Burns, NY, (516) 746-2310

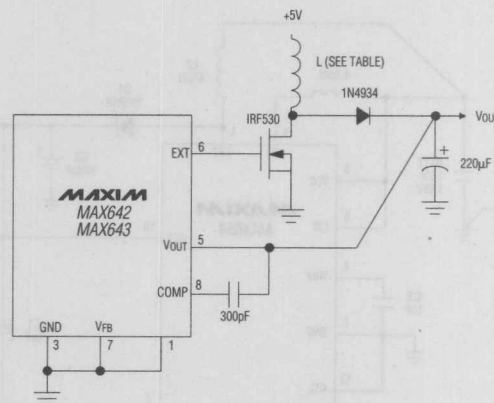


Figure 1-2.

The output voltage limits of the MAX6XX series DC-DC converters can be exceeded once an external FET or transistor with an adequate voltage rating is used as the switch. Here a +12V input is converted to +50V at 50mA by adding an IRF530 N-channel FET which has a voltage rating of 100V. The circuit differs from the basic MAX641 hookup in that an external resistor divider must provide the feedback signal to the V_{FB} input and that chip power comes from the +12V input via the V_{OUT} pin.

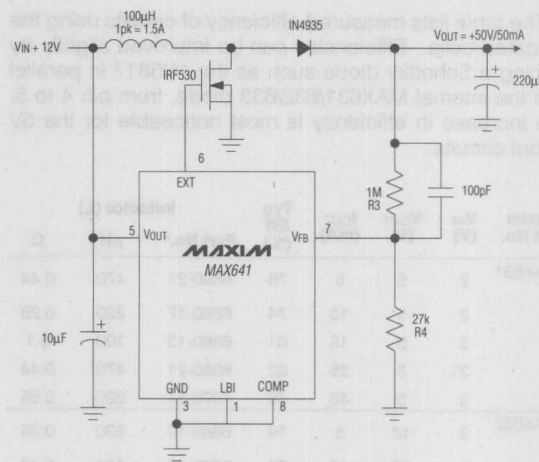


Figure 1-3.

Minimum Component Low Voltage DC-DC Converter

The MAX654 generates 5V at 40mA from a single alkaline battery that has discharged down to 1.2V. Output current vs. input voltage for several values of L2 are shown in the graph. At lower load currents operation continues at even lower battery voltages. When supplying 10mA from its five volt output, this circuit will typically run for 40 continuous hours when powered from a single alkaline AA cell.

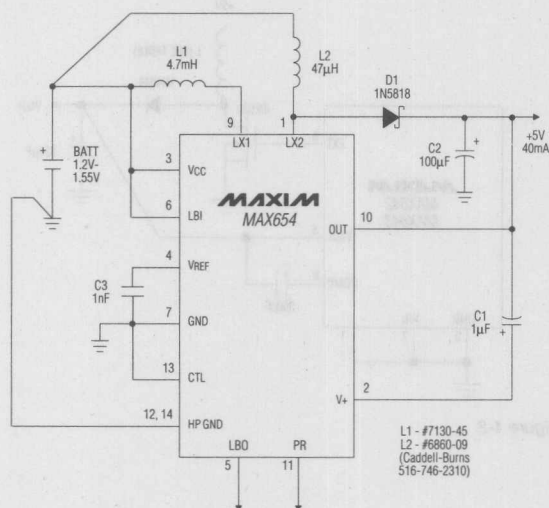


Figure 1-4.

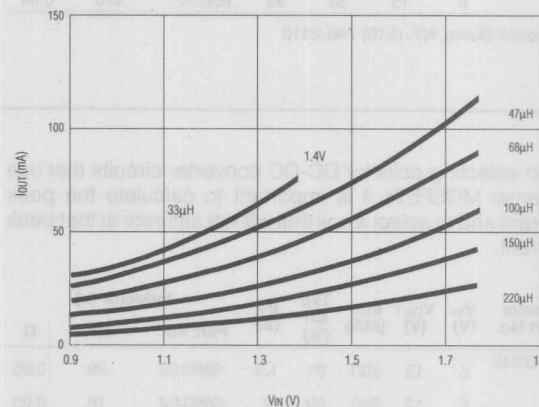


Figure 1-5.

The MAX656 generates 5V at 250mA from a single cell input. Output current vs. input voltage for several values of L2 are shown in the graph. An external IRF541 N-channel MOSFET acts as the main power switch. A small secondary DC-DC converter in the MAX656 generates 12V at low current so that the MOSFET operates with lowest on resistance and highest conversion efficiency. At reduced output current the circuit will operate down to 0.9V input.

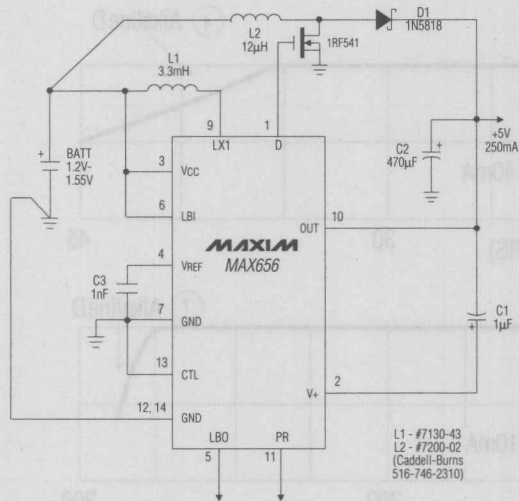


Figure 1-6.

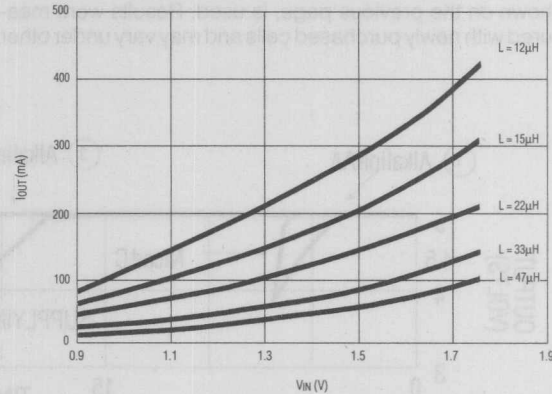


Figure 1-7.

Positive output step-up and step-down DC-DC converters have a common limitation in that neither can handle input voltages which may be both greater than or less than the output. For example, when converting a 12V sealed lead acid battery to a regulated +12V output, the battery voltage may vary from a high of 15V down to 10V.

By using a MAX641 to drive separate P- and N-channel MOSFETs, both ends of the inductor are switched to allow noninverting buck/boost operation. A second advantage of the circuit over most boost-only designs is that the output goes to 0V when SHUTDOWN is activated. A drawback is that efficiency is not optimum because 2 MOSFETs and 2 diodes increase the losses in the charge and discharge path of the inductor. The circuit delivers +12V at 100mA at 70% efficiency with an 8V input.

Step Up/Down DC-DC Converter

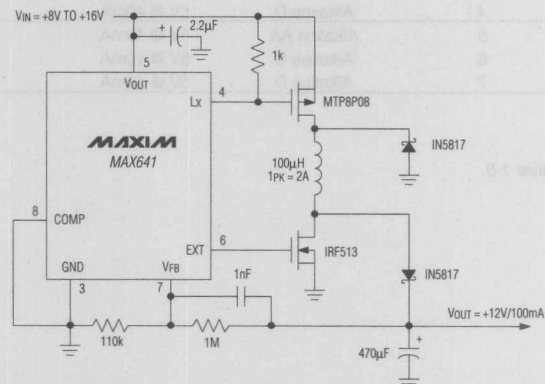
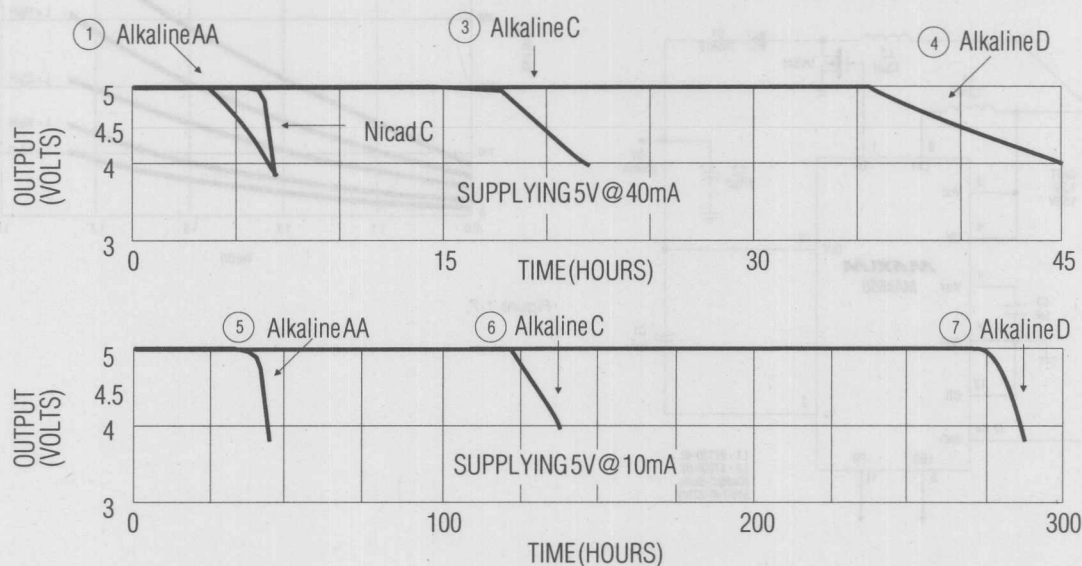


Figure 1-11.

These graphs show typical hours of operating life for a number of single cell alkaline batteries when powering a MAX654 DC-DC converter. The typical application circuit, shown on the previous page, is used. Results were measured with newly purchased cells and may vary under other

conditions. Output load current, battery type, and L2 inductor value are listed for each curve. End-of-life occurs when the MAX654 output falls to 4.5V. The cell voltage at which this occurs and the total Watt-Hours obtained from each battery are also indicated.



TRACE	BATTERY	OUTPUT	BATTERY LIFE (HOURS)	END OF LIFE BATT. VOLTAGE	POWER INDUCTOR	ENERGY DELIVERED
1	Alkaline AA	5V @ 40mA	5	1.04V	63μH	1.0W-Hrs.
2	NiCad C	5V @ 40mA	7	1.1V	47μH	1.4W-Hrs.
3	Alkaline C	5V @ 40mA	20	1.01V	39μH	4.0W-Hrs.
4	Alkaline D	5V @ 40mA	40	1.0V	39μH	8.0W-Hrs.
5	Alkaline AA	5V @ 10mA	43	0.77V	114μH	2.15W-Hrs.
6	Alkaline C	5V @ 10mA	134	0.805V	150μH	6.7W-Hrs.
7	Alkaline D	5V @ 10mA	274	0.932V	157μH	13.7W-Hrs.

Figure 1-8.

You can produce a regulated 5V output from a 1.5V battery cell by using the set-up DC-DC-converter circuit shown. The circuit can operate with V_S as low as 1V, but it requires at least 1.5V to start. The output can deliver 100mA when V_S is 1.5V or 1.7A at 70% minimum efficiency when V_S is 3V.

Supply voltage for the switching regulator IC₁ appears first at pin 4 (start-up mode) and then at its own V_{OUT} terminal, pin 5. The chip includes an oscillator, bandgap reference, three voltage comparators, a catch diode, and associated control circuitry. An internal MOSFET lets you implement low-power applications; higher power calls for an external device: Q1 in Figure 1. The on-chip oscillator provides a 55kHz square-wave drive to both the internal and external MOSFET.

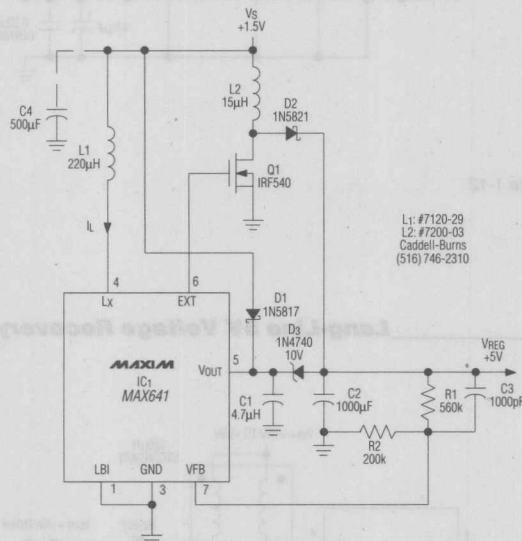


Figure 1-9.

When Q1 turns off, current through inductor L2 drives the drain-node voltage higher. Similarly, current through L1 drives the voltage at pin 5 higher when the internal MOSFET turns off. This action generates two independent voltages, each higher than V_S ; Q1 and L2 generate sufficient overhead voltage to enable the regulator chip to produce a regulated 5V output, and the internally generated voltage ensures adequate gate drive to Q1. The internal voltage, clamped by the 10V zener diode D3, ranges from 10V (turn-on) to 15V (normal operation). Q1's resulting $R_{DS(ON)}$ is only 0.085Ω .

Resistors R1 and R2 determine the regulated output level. For V_{REG} outputs other than 5V, set

$$R_1 = R_2 \left(\frac{V_{OUT}}{1.31} - 1 \right)$$

TABLE 1. OBTAINABLE VALUES OF $I_{OUT\ MAX}$

V_S	L2		
	15µH	27µH	50µH
1.5V	100mA	48mA	30mA
2.0V	200mA	95mA	60mA
2.5V	360mA	160mA	100mA
3.0V	1.7A	1.5A	1.25A

You choose an R2 value in the range from $10k\Omega$ to $10M\Omega$.

For low values of V_S , losses in the internal and external diodes and the Q1 inductor sharply limit the maximum output current. The following design equations let you determine component values while calculating this current. First, Q1 must be able to handle the peak current I_{PK} of inductor L2:

$$I_{PK} = \frac{V_{STON}}{L_2}$$

where $t_{ON} = 0.55/f_{OSC}$. For this circuit, then $I_{PK} = 1.07A$.

The circuit loss V_{LOSS} is

$$V_{LOSS} = I_{PK}(R_{DS(ON)} + 2R_{L2}) + V_{D2}$$

where $t_{ON} = R_{L2}$ is the DC resistance of L2 and V_{D2} is the forward voltage drop of D2. For this circuit $V_{LOSS} = 0.56V$. The output current is

$$I_{OUT} = \frac{0.5 (L_2) I_{PK}^2 f_{OSC}}{V_{REG} - (V_S - V_{LOSS}) - I_{L1}}$$

Therefore, $I_{OUT} = 103mA$ for the circuit shown. Table 1 shows the output currents you can obtain for various values of V_S and L2. The corresponding conversion efficiencies range from 70 to 85%.

A regulated 5V output is obtained from 4 Alkaline or NiCad cells using fewer parts than other buck-boost type converters. The circuit steps down to 5V when the batteries are new (about 6V for Alkaline and 5.4V for NiCad), but also steps up to 5V as the cells discharge and the input drops to 4V and below. Transformers and the more complex buck-boost conversion topologies are avoided by connecting the negative terminal of the battery to the circuit's +5V output and using an inverting topology. This battery connection is not a problem for many portable and hand-held products because the batteries can be treated as a floating source.

The circuit in the figure uses an inverting DC-DC converter IC, the MAX635, to generate what it sees as a negative output voltage. The chip's negative output and ground are then swapped so that a +5V output is supplied with respect to the MAX636's V- input (Pin 1). This appears at GND (Pin 4 on the MAX636). A low cost (about \$1) external P-channel MOSFET and driver IC allow increased inductor current so that up to 200mA can be supplied near the end of battery life. For loads below 20mA, the external FET and the driver IC can be omitted if a 330μH inductor (Caddell-Burns #7070-31) is substituted for the one in the figure. In that case, Lx (Pin 5) connects directly to the coil.

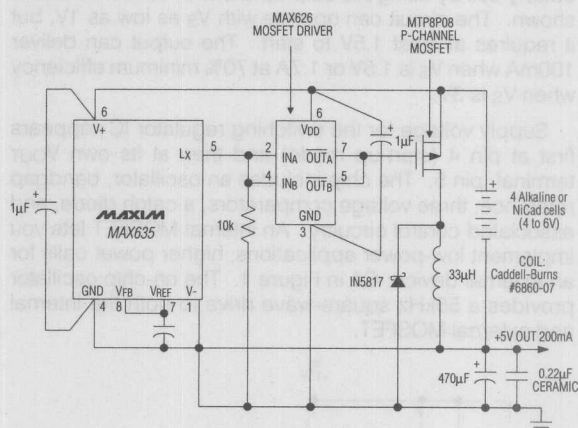


Figure 1-12.

Long-Line 5V Voltage Recovery

This circuit provides a unique solution to a common system-level power distribution problem: When the supply voltage to a remote board must traverse a long cable, the voltage at end of the line sometimes drops to unacceptable levels. This "+5V to +5V" converter addresses this by taking the reduced voltage at the end of the supply line and boosting it back to +5V. This can be especially useful in remote display devices such as some point-of-sale (POS) terminals where several meters of cable may separate the terminal from the read-out. A MAX631 and a small transformer restore the 5V to 4.5V input back to 5V. The 3.2/1 turns ratio of the transformer allows the MAX631 to provide more than its usual output current, without an external MOSFET, at these relative low operating voltages. Output current is 5V at 150mA with a 4.5V input.

* The MAX631 also makes use of the reflected voltage in the transformer primary to generate a higher supply voltage of about +9V for itself at V_{OUT} . By operating at 9V rather than 5V, the on resistance of L_x is reduced.

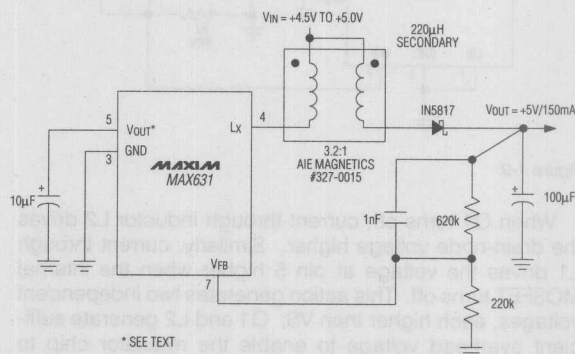


Figure 1-13.

Maxim Part No.	V _{IN} (V)	V _{OUT} (V)	I _{OUT} (mA)	Typ Eff (%)	I _{IN} (A)	Part No.*	μH	Ω
MAX638	7-9.5	5	35	92	200	7070-27	150	0.4
	8-9.5	5	55	89	200	7070-27	150	0.4
	10-14	5	50	92	300	7070-30	270	0.6
	12	5	60	92	250	7070-30	270	0.6
	12	5	75	89	300	7070-28	180	0.5

* Caddell-Burns, NY, (516) 746-2310

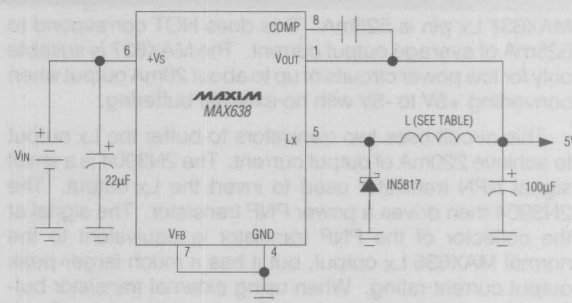


Figure 1-14.

Low Power Inverters

Maxim Part No.	V _{IN} (V)	V _{OUT} (V)	I _{OUT} (mA)	Typ Eff (%)	Inductor (L)		
					Part No.*	μH	Ω
MAX635	+3	-5	5	60	6860-19	330	0.35
	+5	-5	25	76	6860-19	330	0.35
	+9	-5	40	79	6860-19	330	0.35
	+12	-5	45	85	6860-21	470	0.40
	+15	-5	50	90	6860-23	680	0.55
MAX636	+5	-12	12	74	6860-19	330	0.35
	+9	-12	30	84	6860-19	330	0.35
	+12	-12	40	89	6860-21	470	0.40
MAX637	+3	-15	2	65	6860-19	470	0.40
	+5	-15	8	77	6860-19	330	0.35
	+9	-15	25	85	6860-19	330	0.35

* Caddell-Burns, NY, (516) 746-2310

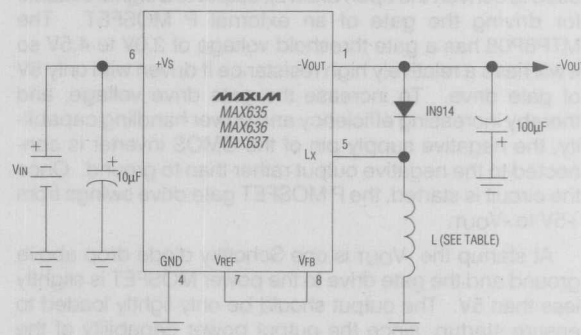


Figure 1-15.

The absolute maximum peak current rating of the MAX637 L_x pin is 525mA. This does NOT correspond to 525mA of average output current. The MAX637 is suitable only for low power circuits of up to about 20mA output when converting +5V to -5V with no external buffering.

This circuit uses two transistors to buffer the L_x output to achieve 220mA of output current. The 2N3904 is a small signal NPN transistor used to invert the L_x output. The 2N3904 then drives a power PNP transistor. The signal at the collector of the PNP transistor is equivalent to the normal MAX636 L_x output, but it has a much larger peak output current rating. When using external transistor buffers, the output voltage is set by an external feedback resistor network; in this case, the 510k Ω and 180k Ω resistors.

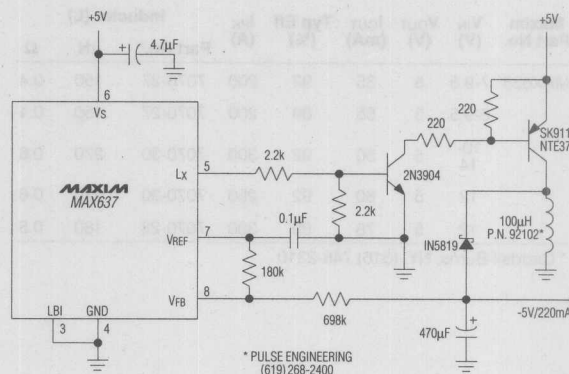


Figure 1-16.

Medium Power Inverters

In this circuit a CMOS inverter such as the MAX626 is used to convert the open drain L_x output to a signal suitable for driving the gate of an external P MOSFET. The MTP8P08 has a gate threshold voltage of 2.0V to 4.5V so it will have a relatively high resistance if driven with only 5V of gate drive. To increase the gate drive voltage, and thereby increasing efficiency and power handling capability, the negative supply pin of the CMOS inverter is connected to the negative output rather than to ground. Once the circuit is started, the P MOSFET gate drive swings from +5V to -V_{OUT}.

At startup the -V_{OUT} is one Schottky diode drop above ground and the gate drive to the power MOSFET is slightly less than 5V. The output should be only lightly loaded to ensure startup, since the output power capability of the circuit is very low until -V_{OUT} is a couple of volts negative.

V _{IN}	-V _{OUT}	I _{OUT}	Efficiency	IC ₁	L ₁
5V	-5V	400mA	70%	MAX635	27μH
5V	-5V	500mA	64%	MAX635	18μH
5V	-12V	150mA	75%	MAX636	27μH
5V	-12V	200mA	70%	MAX636	18μH

Notes:

18mH Coil = Caddell-Burns (Mineola, NY) Model 6860-04
27mH Coil = Caddell-Burns Model 6860-06

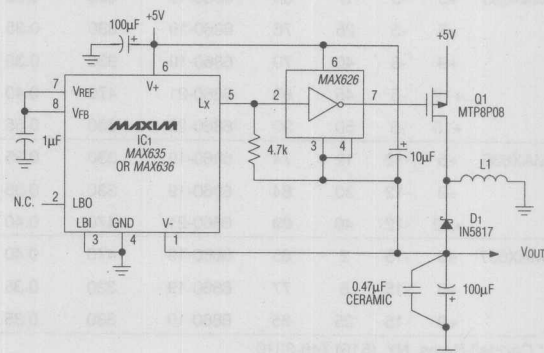


Figure 1-17.

+5V to -24V at 40mA

Similar to the preceding circuit, the 2N4407 PNP transistor is a buffered replica of the MAX637 Lx output. The 2N4407, though, has a high breakdown voltage and can be used to generate a -24V output. The -24V output does not appear directly on any pin of the MAX637 since it is sensed via the 1.5MΩ external feedback resistor.

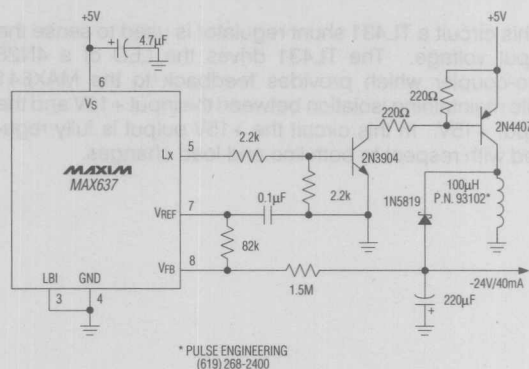


Figure 1-18.

Telecom -48 to 5V at 0.5A

The small current consumption of a MAX641 allows it to be biased at a -48V rail with a shunt zener diode so that it can convert -48V to +5V. This is a common requirement in telecom systems where logic circuitry must be powered from the central office battery voltage.

A small high voltage PNP transistor level shifts a feedback signal from the +5V output down to the MAX641, who ground pin (pin 3) is tied to the -48V input. The chip is biased this way so that EXT can directly drive an N-channel MOSFET to switch the inductor to -48V. This way the circuit operates much like a step-up DC-DC converter. The 330pF capacitor provides feedforward compensation to stabilize the regulator's control loop.

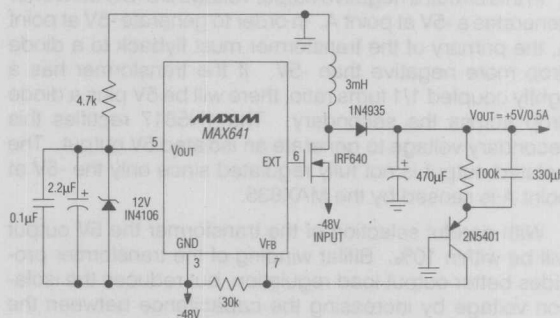


Figure 1-19.

In this circuit a TL431 shunt regulator is used to sense the output voltage. The TL431 drives the LED of a 4N28 opto-coupler which provides feedback to the MAX641 while maintaining isolation between the input +12V and the output +15V. In this circuit the +15V output is fully regulated with respect to both line and load changes.

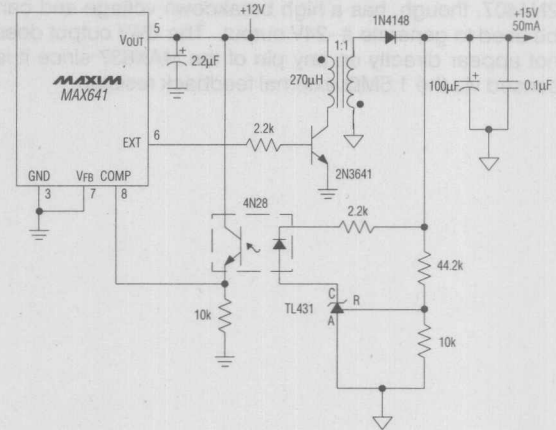


Figure 1-20.

5V to Isolated 5V at 20mA

In this circuit a negative output voltage DC-DC converter generates a -5V at point A. In order to generate -5V at point A, the primary of the transformer must flyback to a diode drop more negative than -5V. If the transformer has a tightly coupled 1/1 turns ratio, there will be 5V plus a diode drop across the secondary. The 1N5817 rectifies this secondary voltage to generate an isolated 5V output. The isolated output is not fully regulated since only the -5V at point A is sensed by the MAX635.

With careful selection of the transformer the 5V output will be within 10%. Bifilar winding of the transformer provides better output load regulation, but reduces the isolation voltage by increasing the capacitance between the primary and secondary. The isolation voltage breakdown is determined by the characteristics of the transformer, not the MAX635.

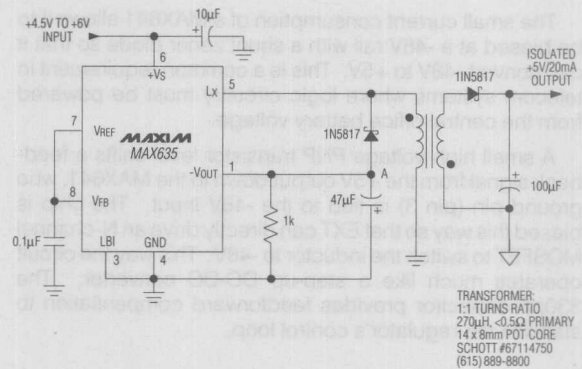


Figure 1-21.

+3V Battery to +5V DC-DC Converter

A common power supply requirement involves conversion of a 2.4 or 3V battery voltage to a 5V logic supply. This circuit converts 3V to 5V at 40mA with 85% efficiency. When I_C (pin 6) is driven low, the output voltage will be the battery voltage minus the drop across diode D1.

The optional circuitry using C1, R3, and R4 lowers the oscillator frequency when the battery voltage falls to 2.0V. This lower frequency maintains the output power capability of the circuit by increasing the peak inductor current, compensating for the reduced battery voltage.

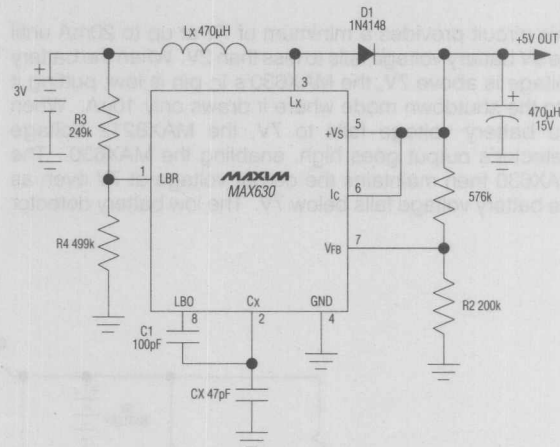


Figure 1-22.

Uninterruptable +5V Supply

In this figure the MAX630 provides a continuous supply of regulated +5V, with automatic switch-over between line power and battery backup. When the line powered input voltage is at +5V, it provides 4.4V to the MAX630 and trickle charges the battery. If the line powered input falls below the battery voltage, the 3.6V battery supplies power to the MAX630, which boosts the battery voltage up to +5V, thus maintaining a continuous supply to the uninterruptable +5V bus. Since the +5V output is always supplied through the MAX630, there are no power spikes or glitches during power transfer.

The MAX630's low battery detector monitors the line powered +5V, and the LBD output can be used to shut down unnecessary section of the system during power failures. Alternatively, the low battery detector could monitor the NiCad battery voltage and provide warning of power loss when the battery is nearly discharged.

Unlike battery backup systems that use 9V batteries, this circuit does not need +12 or +15V to recharge the battery. Consequently, it can be used to provide +5V backup on modules or circuit cards which only have 5V available.

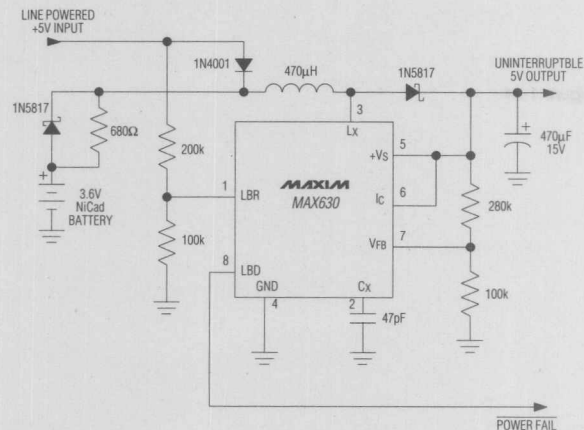


Figure 1-23.

This circuit provides a minimum of 7V at up to 20mA until the 9V battery voltage falls to less than 2V. When the battery voltage is above 7V, the MAX630's I_C pin is low, putting it into the shutdown mode where it draws only 10 μ A. When the battery voltage falls to 7V, the MAX8212 Voltage Detector's output goes high, enabling the MAX630. The MAX630 then maintains the output voltage at 7V even as the battery voltage falls below 7V. The low battery detector

(LBD) is used to decrease the oscillator frequency when the battery voltage falls to 3V. This maintains the output current capability of the circuit at low voltage.

Note that this circuit (with or without the MAX8212) can be used to provide 5V from 4 alkaline cells. The initial voltage is approximately 6V, and the output is maintained at 5V even when the battery voltage falls to less than 2V.

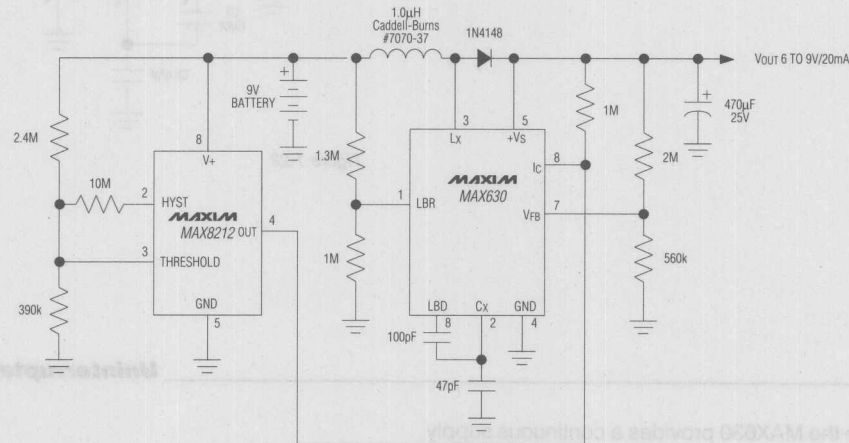


Figure 1-24.

MAX630 in this figure to provide a dual tracking $\pm 12V$ output from a 9V battery. The reference for the -12V output is derived from the positive output via R3 and R4.

battery voltage by reducing the oscillator frequency, via LBR, when V_{BATT} falls to 8.5V

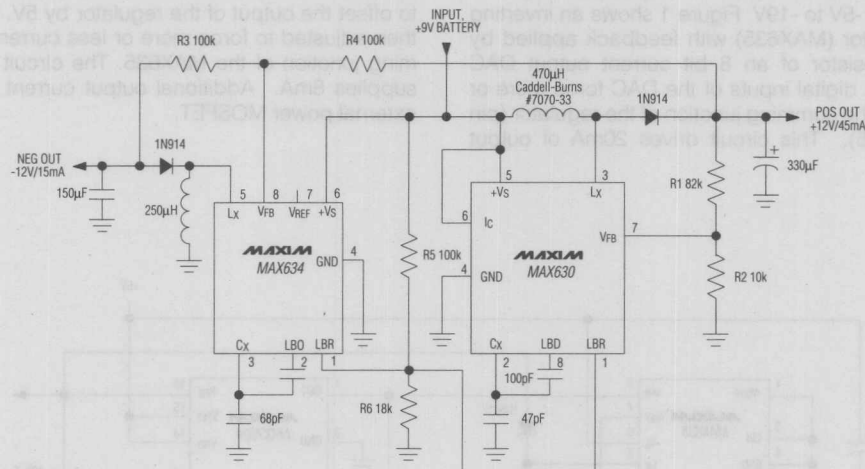


Figure 1-25.

5V from Battery Input in "Positive Ground" Circuits

In small battery powered devices, the task of converting the battery voltage to usable levels is sometimes compounded by constraints in the design and packaging of the finished product. In one such case, circuit requirements dictated that the battery positive connection be common to both the battery input and the load. Input power is from 2 AA batteries. The circuit must supply 5V at 4mA and also be able to start with an input voltage as low as 2.1V. This allows full operation at an end-of-life potential of 1.05V per cell.

High efficiency and low operating voltage are accomplished by using a MAX638 CMOS "step-down" DC-DC converter in the somewhat convoluted configuration shown in the figure. Current flows in the 470μH coil when the internal switch at Lx turns on. After roughly 10μs this switch turns off and inductor current is drawn from the negative output terminal of the circuit via the 1N5817 Schottky rectifier. The 5V output is well regulated since the MAX638 controls the operation of the Lx switch so that 5V is maintained between its VOUT and GND pins.

When supplying a 5V output, the circuit itself typically consumes only 170μA from the battery input. In addition, conversion efficiency is maintained at low input voltages. While supplying 5V at 4mA, total current drawn from the battery at 2.1V is only 11.5mA. Thus typical conversion efficiency at end-of-life voltages is still over 80%.

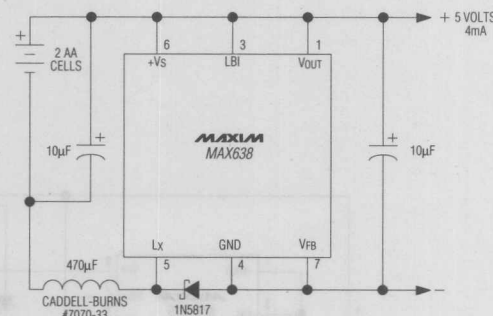


Figure 1-26.

A simple modification to the feedback network of an inverting switching regulator allows the user to adjust the negative output. This is useful in LCD display applications where the user can adjust the display contrast digitally. The two schemes shown allow an adjustable output of either 0 to -5V or -5V to -19V. Figure 1 shows an inverting switching regulator (MAX635) with feedback applied by the feedback resistor of an 8 bit current output DAC (MAX7624). The digital inputs of the DAC force more or less current into the summing junction of the regulator (pin 8 of the MAX635). This circuit drives 20mA of output current.

Figure 1-28 shows how a dual 8 bit current output DAC (MX7528) can extend the output voltage range by using the two DACs in parallel. The feedback resistor of the first DAC is tied to the regulator output. The feedback resistor of the second DAC is tied to the reference (the 5V power supply) to offset the output of the regulator by 5V. The DACs are then adjusted to force more or less current into the summing junction of the MAX635. The circuit in Figure 1-28 supplies 8mA. Additional output current will require an external power MOSFET.

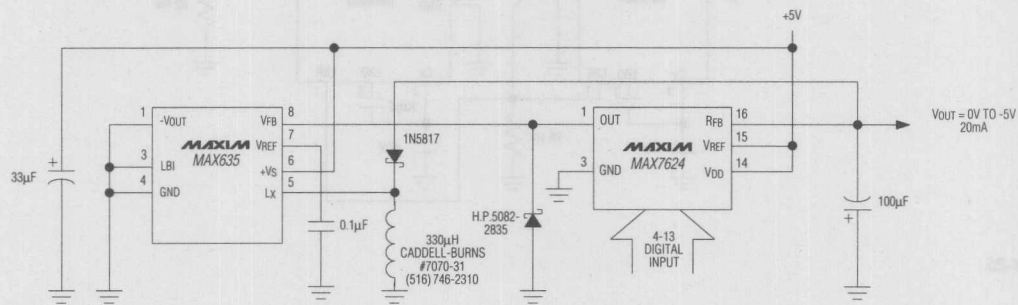


Figure 1-27.

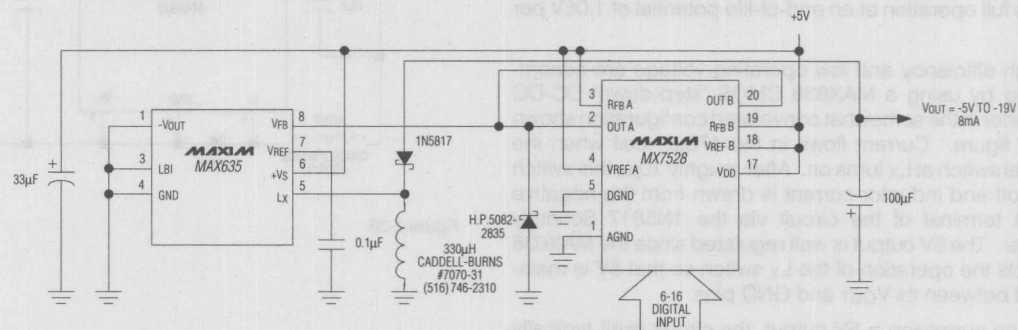


Figure 1-28.

Switching Regulator Makes High Current Flasher

The following circuit uses the internal power MOSFET of a CMOS switching regulator to drive an incandescent light bulb in a highway flasher which operates off of a 6V lantern battery. The CMOS regulator also has the advantage of 1 micro-amp maximum shutdown current. Shutdown can be accomplished by connecting Ic, pin 6, to a voltage lower than 0.2 volts. A simple voltage divider consisting of a 5.1M Ω resistor, R1, and a photo sensitive resistor, R2, can provide the input necessary to turn the flasher off during the daytime and activate it at night.

The MAX630 CMOS switching regulator was designed to operate at a 50kHz rate with a 50% duty cycle. Regulation occurs by skipping cycles when the voltage divided output exceeds the internal 1.3V reference voltage. This regulator has the option of adding an external capacitor to the Cx, pin 2, to slow down the frequency of the internal oscillator. By adding 1 μ F capacitor to this pin the frequency drops to about 1 Hertz. The internal N-MOS power transistor is rated at 1/2 amp peak current which is sufficient for many 6V incandescent light bulbs.

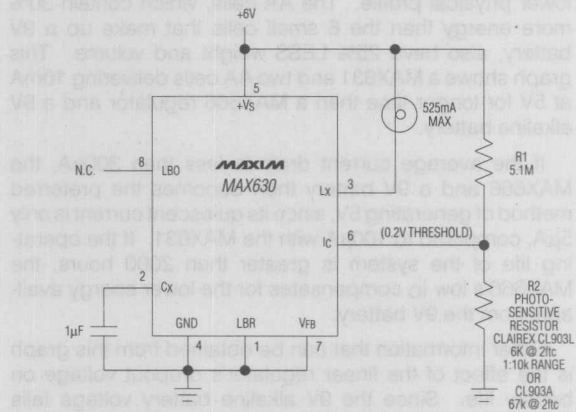
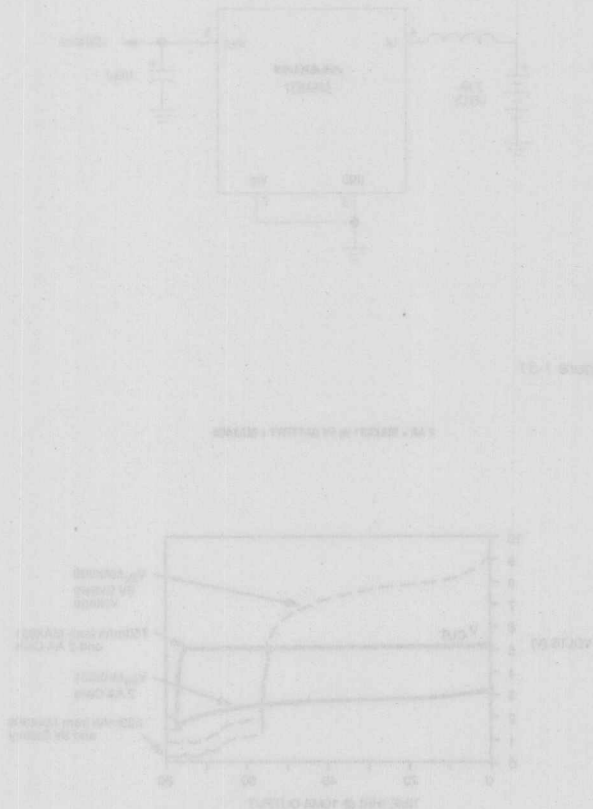


Figure 1-29.



Battery Comparison: 9V Battery vs. 2 AA Batteries

A MAX631 DC-DC converter, a small inductor, and two AA penlight cells can replace a 9V transistor battery, increasing battery life while simultaneously allowing a lower physical profile. The AA cells, which contain 30% more energy than the 6 small cells that make up a 9V battery, also have 25% LESS weight and volume. This graph shows a MAX631 and two AA cells delivering 10mA at 5V for longer time than a MAX666 regulator and a 9V alkaline battery.

If the average current drain is less than 300 μ A, the MAX666 and a 9V battery then becomes the preferred method of generating 5V, since its quiescent current is only 5 μ A, compared to 100 μ A with the MAX631. If the operating life of the system is greater than 2000 hours, the MAX666's low I_Q compensates for the lower energy available from the 9V battery.

Other information that can be obtained from this graph is the effect of the linear regulator's dropout voltage on battery life. Since the 9V alkaline battery voltage falls rather rapidly near end-of-life, the 0.6V dropout voltage of the MAX666 has only a minimal effect. For this reason regulators with lower dropout voltage but higher quiescent current than the MAX666 are frequently a poor tradeoff for maximum battery life with alkaline cells.

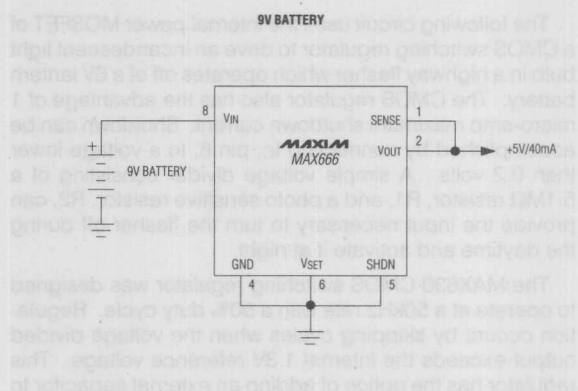


Figure 1-30.

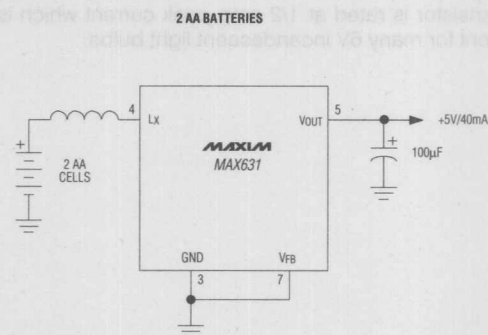


Figure 1-31.

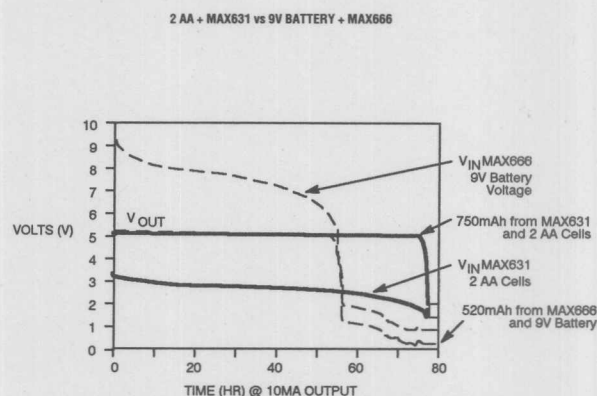


Figure 1-32.

Maxim's DC-DC converters/switching regulators employ an operating principle often termed "flyback", where an inductor (coil) alternately stores and releases energy which is directed to a load in a controlled manner. The circuits are so named because the voltage on the coil inverts or "flies back" when power is removed on each switching cycle. A well known example of this type of circuit operates in automobile ignitions, to develop high spark voltages from a 12V battery input.

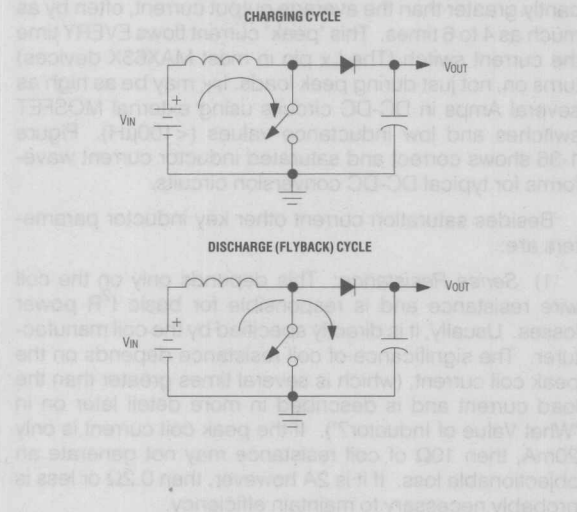


Figure 1-33.

In spite of the fact that flyback circuits do use inductors (and occasionally transformers) they are not difficult to understand, at least in a qualitative way, without an intense mathematical examination. When current flows in an inductor, energy is stored in an "induced" magnetic field in the area surrounding the coil. This field also generates a "counter E.M.F." which opposes the applied current. This is why inductors attempt to maintain constant current flow through themselves (as a compliment to how capacitors resist a change in voltage on their plates).

When a fixed voltage is applied to an inductor, the current rises linearly as a function of the applied voltage and the coil inductance. If the voltage is applied indefinitely, the current, in a theoretical inductor rises to infinity. In a real-life coil, the current rises until it is limited by the resistance present in the coil, switch, and elsewhere in the circuit. Sometimes the current rises until the saturation limit of the coil's core material is exceeded. When saturation occurs, the coil ceases to be an inductor and the current may then rise uncontrollably. Inductor saturation should be avoided for this reason (See "Inductor Saturation" on next page).

In a typical DC-DC converter or switching regulator circuit, a voltage is first applied to a coil for a controlled time (typically 10 μ s in MAX6XX DC-DC converters). This induces a current which rises linearly until the voltage is removed. At that point the coil current, which resists change, looks for some other place to flow. A steering or "catch" diode directs this current to the output. The key (in step-up converters) to getting a higher output than input voltage, is that the coil voltage rises to the level that allows the current to keep flowing. The circuit output can then be regulated by monitoring the output voltage and controlling the switch which applies power to the coil.

The particular example describes a step-up or "boost" converter, however inverting and step-down circuits are no more complex. They differ only in the positions of the three basic components: coil, switch, and diode. The three basic configurations: Step-Up, Step-Down, and Inverting, are shown in Figure 1-34.

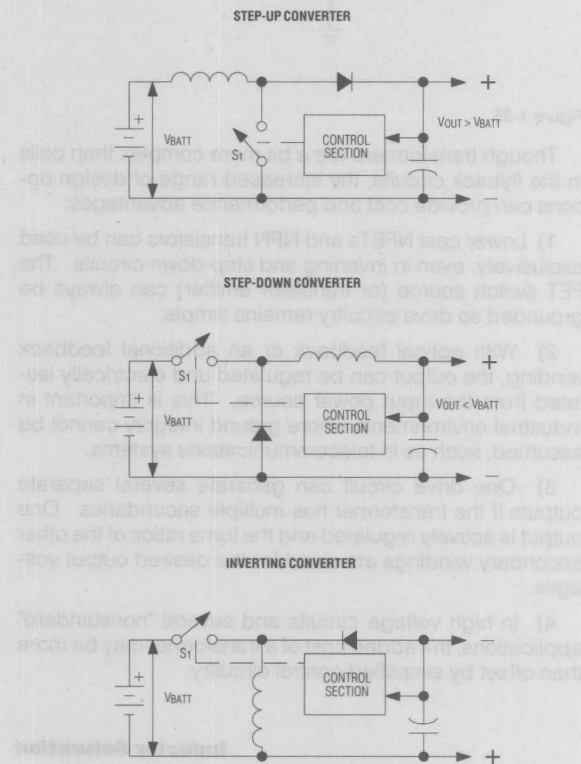


Figure 1-34.

inductors. Transformers are also frequently used. Flyback transformer operation is very similar to the inductor example above. The only operating difference occurs during the period when current in the primary circuit is interrupted. Since no current path or steering diode is provided in the primary circuit at that point in time, the flyback current flows in the secondary winding to the output.

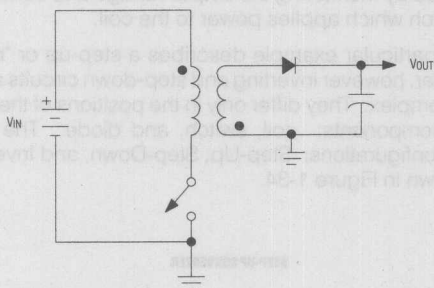


Figure 1-35.

Though transformers are a bit more complex than coils in the flyback circuits, the increased range of design options can provide cost and performance advantages:

- 1) Lower cost NFETs and NPN transistors can be used exclusively, even in inverting and step-down circuits. The FET switch source (or transistor emitter) can always be grounded so drive circuitry remains simple.
- 2) With optical feedback or an additional feedback winding, the output can be regulated and electrically isolated from the input power source. This is important in industrial environments where ground integrity cannot be assumed, such as in telecommunications systems.
- 3) One drive circuit can generate several separate outputs if the transformer has multiple secondaries. One output is actively regulated and the turns ratios of the other secondary windings are sized for the desired output voltages.
- 4) In high voltage circuits and several "nonstandard" applications, the added cost of a transformer may be more than offset by simplified control circuitry.

Inductor Saturation

Not every inductor is appropriate for DC-DC conversion circuitry. Even with the proper inductance value an "unknown" inductance may still saturate if it cannot handle the required current. Although the inductance value of several types of coils, such as RF chokes, air core inductors, and noise filtering components frequently fall in the appropriate

inductor, i.e. the mechanism which limits the rate of current rise breaks down. Energy is no longer being stored in the coil's magnetic field. The current, limited only by the supply voltage and the resistance in the charging path, rises to excessive (possibly destructive) levels and most of the input power is lost as heat.

A coil will not saturate as long as its charging current does not exceed its current rating. However, in most DC-DC designs the peak inductor current (I_{PK}) is significantly greater than the average output current, often by as much as 4 to 6 times. This "peak" current flows EVERY time the current switch (The L_X pin in most MAX63X devices) turns on, not just during peak loads. I_{PK} may be as high as several Amps in DC-DC circuits using external MOSFET switches and low inductance values ($<100\mu H$). Figure 1-36 shows correct and saturated inductor current waveforms for typical DC-DC conversion circuits.

Besides saturation current other key inductor parameters are:

- 1) *Series Resistance*: This depends only on the coil wire resistance and is responsible for basic I^2R power losses. Usually, it is directly specified by the coil manufacturer. The significance of coil resistance depends on the peak coil current, (which is several times greater than the load current and is described in more detail later on in "What Value of Inductor?"). If the peak coil current is only 20mA, then 10Ω of coil resistance may not generate an objectionable loss. If it is 2A however, then 0.2Ω or less is probably necessary to maintain efficiency.
- 2) *Core loss*: This is not well defined by coil manufacturers and is usually absent from coil data sheets. Toroids and pot cores typically (but not exclusively) have lower losses than cylindrical types, but in low power circuits the efficiency differences usually do not justify the cost difference. In high power circuits toroids are more attractive because of typically higher current ratings. Highest efficiency with cylindrical coils is when ferrite core material is used. In less demanding applications, a lower cost alternative for both toroids and cylindrical coils is powdered iron, but these tend to be larger for a given current rating and inductance.

Due to the low voltage drop and consequently the

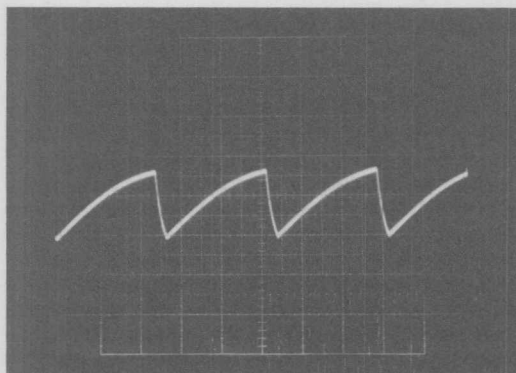
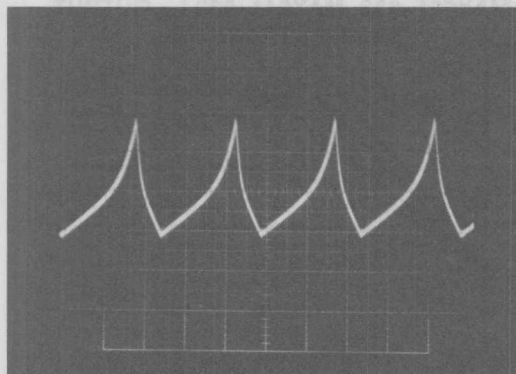
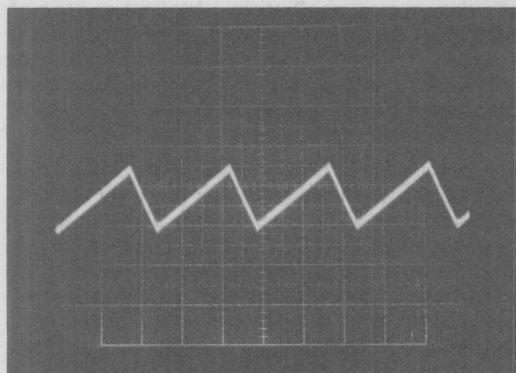


Figure 1-36.

Typical Inductor Current Waveforms (200mA/div, 2 μ s/div)

CMOS DC-DC converters are generally used in low power applications where efficiency is of prime importance. The following table lists the typical efficiency and methods for minimizing each effect.

Switch Resistance - Operating a MAX981-643 converter at the highest possible supply voltage (up to the maximum 16.5V rating) results in the lowest internal switch resistance. The effect of supply voltage on switch resistance for several MAX981-643 devices is shown in Figure 1-37. For lowest switch resistance, an external MOSFET can be easily added to many devices. Logic level FETs, which need only 5V of gate-source voltage to turn on, are preferred for many low voltage applications.

Normal Operation -
Linear charge and discharge slopes

MAX981-643 I_L OUTPUT CHARACTERISTICS



Saturation -
Non-linear increase in inductor current near peaks

The output characteristics of the internal I_L switch in MAX981-643 DC-DC converters are shown in the two graphs of Figure 1-37. The MAX981-643 plot is for an N-channel output device while the MAX981-643 plot is for a P-channel device. Both graphs show that the external saturation current for each device is relatively low and its on resistance is high when the clip's supply voltage is close to V_{DS} (the device's V_{DS} is less). The increase in slope as V_{DS} increases, which corresponds to lower on resistance, shows how conversion efficiency is improved when the clip is powered from the highest available supply voltage.

Inductor Resistance - Select lowest possible DC resistance. This may conflict with other requirements. Inductor resistance also can be reduced by using a low resistance wire or a low resistance wire. The inductor is typically used for low power applications. The inductor is used for low power applications.

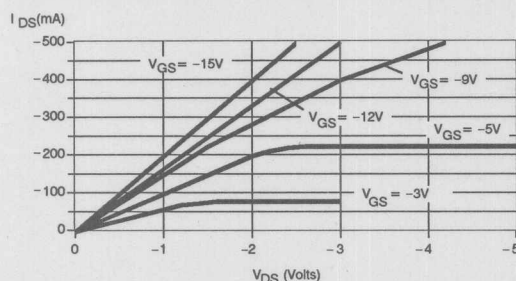
Inductor Core Loss - This can be reduced by using a core with low core loss. The inductor is used for low power applications. The inductor is used for low power applications.

Maximizing Efficiency

CMOS DC-DC converters are generally used in low power applications where efficiency is of prime importance. In the following text the major causes of energy loss, and methods for minimizing each, are listed.

Switch Resistance - Operating a MAX6XX DC-DC converter at the highest possible supply voltage (up to the maximum 16.5V rating) results in the lowest internal switch resistance. The effect of supply voltage on switch resistance for several MAX6XX devices is shown in Figure 1-37. For lowest switch resistance, an external MOSFET can be easily added to many devices. Logic level FETs, which need only 5V of gate-source voltage to turn on, are recommended for many low voltage applications.

MAX634-638 L_x OUTPUT CHARACTERISTICS



MAX631-633, MAX641-633 L_x OUTPUT CHARACTERISTICS

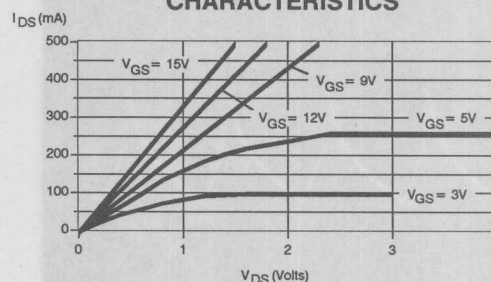


Figure 1-37. Internal switch characteristics for several MAX63X devices. V_{GS} in the graphs is equivalent to the input voltage for the device.

The output characteristics of the internal L_x switch in MAX series DC-DC converters are shown in the two graphs of Figure 1-37. The MAX631-33, MAX641-643 plot is for an N-channel output device while the MAX634-638 graph is for a P-channel device. Both graphs show that the switchers saturation current for each device is relatively low and its on resistance is high when the chip's supply voltage (equivalent to V_{GS} in the graphs) is 5V or less. The increase in slope as V_{GS} increases, which corresponds to lower on resistance, shows how conversion efficiency is improved when the chip is powered from the highest available supply voltage.

Inductor Resistance - Select lowest possible DC resistance. This may conflict with size limitations in some applications, since coil wire resistance is inversely related to size. Fortunately, the low (<500μH) inductance values typically called for in low power DC-DC converter designs do tend toward low series resistance values.

Inductor Core Losses - This can be reduced with larger core sizes and/or lower loss core material. (See "Inductor Saturation" in previous text)

Diode Losses - Schottky diodes, like the 1N5818, provide the lowest forward voltage drop, and consequently the best efficiency in most applications. Alternatives are high speed silicon switching rectifiers such as 1N4935 or, in low power circuits (<10mA), 1N4148 signal diodes. Rectifier switching speed is important in DC-DC conversion circuits so conventional power supply rectifiers, like 1N4001, should not be used.

Quiescent Current - This is especially important in low power applications, particularly those powered from primary batteries (see "Summary of Battery Chemistries"). If the output current of a DC-DC converter is only a few mA, then the efficiency cannot be greater than 50% if the conversion circuit itself uses that much current to operate. The best choice is to use devices with low operating current. Most MAX6XX devices use only 100's of μA.

Operating current is also reduced by selecting maximum values for feedback and pullup resistors when they are used.

Switching Time - The power switch in any DC-DC conversion circuit dissipates the most power during the instant that it turns on or off. By making the turn-on and turn-off times as fast as possible, efficiency is optimized. When driving external FETs, the rise and fall time of the gate drive signal should also be short. Many MAX series parts drive external FETs directly (or with minimum circuitry), however especially large power MOSFETs, with high gate-to-source capacitance (1000pF is common), may need low impedance gate drivers. This is so that the gate-source capacitance does not slow the drive waveform and also the switching time. An external power FET driver from the MAX626 family accomplishes this.

Low Power Efficiency vs. Output Current

One advantage of CMOS in low power DC-DC conversion is that for very low load currents, the efficiency remains high. As shown in the graph of Figure 1-37, even with a 1mA load, the circuit's quiescent current does not impact efficiency.

EFFICIENCY VS OUTPUT CURRENT (MAX 630, 3 volts to 5 volts)

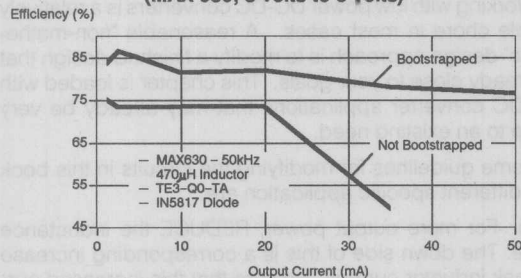


Figure 1-37. Efficiency vs. output current for a MAX630 step-up converter. "Bootstrapped" means that the MAX630 chip is powered from the circuit output voltage rather than the battery input. Either connection is possible but bootstrapping improves efficiency.

Also shown in the graph is the improvement in output current and efficiency resulting from using a "bootstrapped" connection where the chip power is supplied from the +5V output rather than the +3V input. The increased chip supply voltage means higher gate drive for the internal N-channel switch. The efficiency is increased because the switch on resistance is reduced. The MAX630 can be connected in either configuration, but most basic MAX DC-DC converters are used in bootstrapped mode for best efficiency.

Hints on Grounds, Bypass Caps, Compensation

Instability in the feedback loop, caused by contaminated ground connections or stray capacitive pickup, can severely limit the performance of an otherwise sound DC-DC converter design. Symptoms of trouble are often high ripple, much poorer than expected efficiency, and "motorboating" or low frequency oscillation. Motorboating occurs when the control loop of the DC-DC converter outputs pulses in periodic clusters (10-20 pulses long) rather than at random intervals. This happens because the loop has been destabilized by one or more of the following items. Figure 1-38 illustrates some general approaches to optimum layout and bypassing.

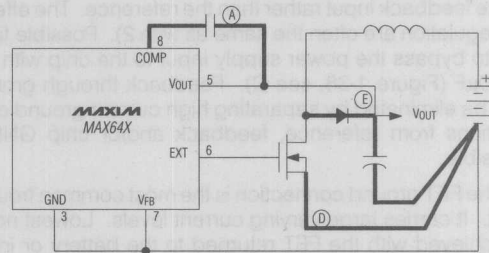
1) Capacitance at feedback input (VFB)

The effect of this capacitance is to delay or "lag" the arrival of feedback information to the regulator. The delay may cause overshoot or instability in the form of "motorboating" (see above). The result is usually seen as high output ripple (100's of mV to Volts) and reduced efficiency.

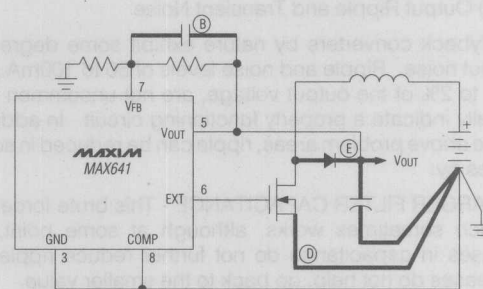
A capacitor (100 to 1000pF) connected between the circuit output and the COMP pin (100 to 1000pF) adds "lead" compensation to reduce ripple and improve the

transient response of the regulating loop (Figure 1-38, see A). This capacitor in effect AC couples additional feedback information around the feedback network to speed up the regulator's response (and reduce motorboating). This may also slightly shift the DC output voltage from its level without compensation.

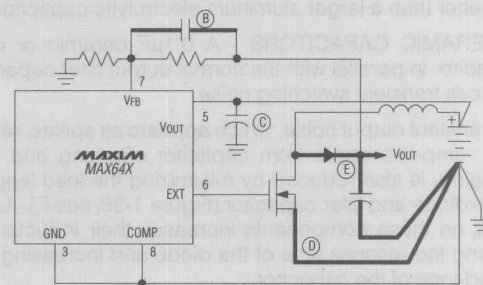
If external resistors are used to set the output voltage via VFB, then the compensation capacitor is connected across the upper feedback resistor (Figure 1-38, see B) and the COMP pin is grounded. When feedback resistors are used, reduce the length of connections at the VFB input to minimize capacitance from this point to GND.



INTERNAL FEEDBACK - BOOTSTRAPPED



EXTERNAL FEEDBACK - BOOTSTRAPPED



EXTERNAL FEEDBACK - NOT BOOTSTRAPPED

Figure 1-38. Optimum connections for typical step-up circuits. The circled letters are referenced in the test, "Hints on Grounds Bypass Caps, Compensation". Step-down and inverting circuits are not shown, but similar steps apply.

2) Ripple or noise coupling to the reference

Injected noise or ripple on the reference typically is seen in some form on the output as well. In particularly unfortunate circumstances it may also destabilize regulation. The cause of this is often poor grounding practice, where a high current (inductor or switch) ground interferes with the regulator's ground and hence its reference. Solutions are to either bypass the reference and/or $+V_S$ (or V_{OUT} , which is the + supply pin on several devices) to GND with a 0.1 to 1 μ F capacitor (Figure 1-38, see C).

3) Feedback Via GND or Supply Input

This is similar to 2) except that ripple and noise couple to the feedback input rather than the reference. The effects on regulation are often the same as with 2). Possible fixes are to bypass the power supply input to the chip with 0.1 to 10 μ F (Figure 1-38, see C). Feedback through ground can be eliminated by separating high current ground connections from reference, feedback and/or chip GND if possible.

The FET ground connection is the most common trouble spot. It carries large varying current levels. Lowest noise is achieved with the FET returned to the battery or input supply via a separate trace or wire (Figure 1-38, see D). If all ground connections must be shared by one trace, make it as wide and short as possible.

4) Output Ripple and Transient Noise

Flyback converters by nature exhibit some degree of output noise. Ripple and noise levels of 50 to 100mA p-p, or 1 to 2% of the output voltage, are not uncommon and usually indicate a properly functioning circuit. In addition to the above problem areas, ripple can be reduced in some cases by:

LARGER FILTER CAPACITANCE - This brute force approach sometimes works, although at some point, increases in capacitance do not further reduce ripple. If increases do not help, go back to the smaller value.

LOWER CAPACITORS - A smaller value filter capacitor with low Equivalent Series Resistance (ESR) may actually do better than a larger aluminum electrolytic capacitor.

CERAMIC CAPACITORS - A 0.1 μ F ceramic or chip capacitor in parallel with the normal output filter capacitor reduces transient switching noise.

Transient output noise, which appears as spikes, rather than ramp-like ripple from capacitor charging and discharging, is also reduced by minimizing the lead lengths at the diode and filter capacitor (Figure 1-38, see E). Long leads on these components increases their inductance, slowing the response time of the diode and increasing the impedance of the capacitor.

Another important characteristic of transient noise is that it often appears to be where it really is not. Before trying to eliminate spikes with capacitors or whatever, verify that the transients are really part of the output waveform. Try different scope ground arrangements to be sure that the observed signal is not a result of an unfortunate ground clip location. Even long probe ground clip leads sometimes

increase the apparent switching noise by picking up radiated signals. A good test is to connect the probe ground to the probe tip (shorting it out) and then touch various circuit ground points. If the same transients are seen, then the probe's ground clip is picking up radiated noise and the clip should be shortened. Winding unused ground lead tightly around the probe tip may also help.

The Easy Way to Low Power DC-DC Converter design

Working with low power DC-DC converters is a relatively simple chore in most cases. A reasonable "non-mathematic" design approach is to modify a finished design that is already close to your goals. This chapter is loaded with DC-DC converter applications that may already be very close to an existing need.

Some guidelines for modifying the circuits in this book to a different specific application are:

1) For more output power, REDUCE the inductance value. The down side of this is a corresponding increase in peak inductor current. Be sure that this increased current doesn't exceed the L_X current rating. If it does, an external transistor or FET, that can handle the higher current, is necessary. Note that the data sheet rating for peak L_X current (I_{PK}) is NOT THE SAME AS OUTPUT CURRENT. (See later section, "What Value of Inductor?") I_{PK} at L_X often will be as much as four to six times greater than output current.

2) If less output power is needed, increasing the inductor value will usually improve efficiency and reduce ripple. This reduces the peak inductor current so switch losses are also less.

3) Changing the output voltage to other than the available fixed outputs in most circuits is usually as simple as adding two feedback resistors (See data sheet for each device). Increasing the voltage will of course mean reduced output current if the inductor remains the same.

Winding inductors and transformers using pot cores and toroids can be very useful when prototyping DC-DC conversion circuits and need not be a painful process. The problem experienced by designers who are unfamiliar with magnetics is that an uncomplicated "working" solution is hard to find in what seems to be an impenetrable mass of specifications in the core manufacturers' catalogs.

Where do you start? Presented here is a short "minimum calculation" procedure for inductor and transformer design based on shortcuts pulled from manufacturers literature. It won't provide the "best" inductor for all applications, but for flyback switching converters which allow some shortcuts, it's a convenient way to designing prototypes and judge the feasibility of a design.

Standard values of inductors are stocking and sampled by several coil manufacturers (See appendix) so once a prototype coil is tried successfully it can often be replaced by a standard product in production. With transformers, winding prototypes is more useful because so few switching transformers are offered as standard products. A homemade prototype can also be a model for the magnetics manufacturer when designing the final production transformer.

"Shortcut" Inductor and Transformer Design

1) Two basic inductor parameters are needed to start:

- a) Inductance - L
- b) Peak coil current - I_{pk}

These are determined from the initial DC-DC converter design. How these values are selected in various circuits is covered in Section 4. Most DC-DC converter applications in Maxim's literature will specify the required inductance and peak current. From the above parameters, calculate the LI^2 product in millijoules ($mH \times Amps^2 = mJ$). This is actually two times the maximum amount of energy that the core must store ($E = LI^2/2$) but is the quantity specified in most pot core and toroid literature.

POT CORE SELECTION GUIDE

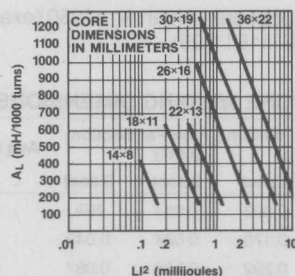


Figure 1-39. This graph determines the smallest core that will work for a given LI^2 product. See Pot Core and Toroid Basics for a detailed explanation.

2) Pick the core size from the Pot Core Selection Guide. Find LI^2 on the X axis and draw a vertical line up from the point to the lowest intersecting diagonal line. Read the inductance factor, A_L , from the Y axis. The diagonal line and the corresponding value from the Y axis represent the smallest core size and the maximum A_L that may be used (A_L is the inductance per turns squared for the core). This means that any core of that size, with an A_L less than the Y axis value, will not saturate. Also, any other core that intersects the LI^2 line is usable if its A_L is less than the Y axis value. Of course if a core with too small an A_L is selected then the needed number of turns may not fit on the core.

In flyback transformers, wire size, resistance, and "fitting" the turns on the core is usually not a problem. This is because the specified inductances are small compared to other types of switching transformers so few turns are needed. This often allows the use of significantly smaller A_L values than provided by the graph, which reduces core losses. This gain however must be weighed against the increased wire losses.

3) The number of turns of wire, N, to be wound on the core for the desired inductance is:

$$N = 31.6 (\sqrt{A_L}), \text{ where } L \text{ is the inductance in } \mu H.$$

4) Knowing how many turns are needed, we then want the largest wire that will fit on the core (within reason) to minimize the DC resistance. The available winding area, A_w , can either be directly found in the data for the core bobbin, or by using the Ferrite Pot Core Winding Dimensions table.

$$T \geq N/A_w$$

T, the turns/cm² from the Wire Table, must be greater than the required number or turns, N, divided by the available winding area, A_w . A wire size with an adequate value for T should be used.

5) Once the wire size is picked, the resistance is checked using data from the Wire Table and the Winding Dimensions table.

$$R = NI_w r_w$$

N is the number of turns, I_w is the average length of a turn for the selected core, and r_w is the resistance/foot of the selected wire. R should be such that no more than 1 or 2% of the total power is lost in the wire resistance. The power lost due to wire resistance in flyback circuits is roughly:

$$P_R = (I_{pk}^2 \times R)/3$$

If the inductor or transformer is extremely small, then a somewhat larger percentage may be allowed. This is not normally a problem in flyback circuits since the inductance and hence the number of turns required is relatively small compared to other converter types. If the resistance is too high, a larger wire size (with lower ohms/foot), and possibly a larger core to accept the larger wire diameter, must be used.

Designing Transformers

Transformers for flyback converters are no more difficult to wind than inductors. The primary winding is designed in the same manner as above and basic turns ratios are used to design the secondary winding(s). The ratios will usually be proportional to or slightly less than the input/output voltage ratios, i.e., 2/1 for a 10V to 5V circuit or 1/3/3 for 5V to $\pm 15V$.

Transformer Example

One application where a transformer is a desirable alternative to an inductor is in this DC-DC converter which generates 5V at 1 Amp from 4 NiCad cells. Since the input voltage varies from 4V to 5.2V neither a step-up nor a step-down converter works over the full input range. Also, the input and output voltages are too low to drive the P-Channel MOSFETs normally used in step-down circuits. A transformer allows us to not only step up or down, but also to use a lower cost N-channel FET grounded source switch. With a transformer we can also cut all power to the load when the converter is shut down, which is something a basic step-up converter is not able to do.

First of all, the required output power, assuming a 0.5V forward diode drop (1N5817), is 5.5W. With a 50kHz clock frequency (MAX641) and a minimum input voltage of 4V, the inductance required, L_p , is:

$$L_p = I_N^2 / (9f_o I_{OUT} (V_{OUT} + V_D)) \\ = 4^2 / (8 \times 50\text{kHz} \times 1 \times (5 + 0.5)) = 7.27\mu\text{H}$$

The peak current in the transformer, calculated using the highest input voltage (5.2V), is:

$$I_{PK} = V_{IN} / (2f_o L) = 7.15\text{ Amps}$$

$$\text{Then } LI^2 = 0.372\text{ millijoules (mJ)}$$

Using the Pot Core Selection Guide, 0.372 millijoules leads us to a 18x11 mm pot core with an A_L value of no more than 330.

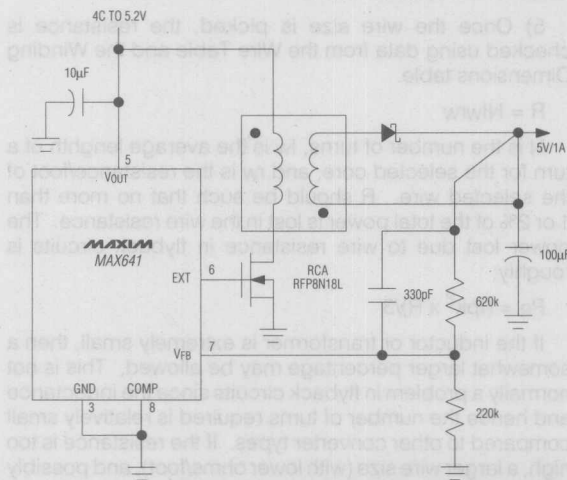


Figure 1-40. DC-DC Transformer Example

WINDING AREA AND LENGTH

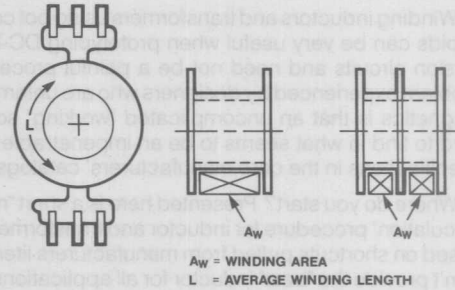


Figure 1-41.

We select a standard core with an A_L of 250. The number of turns needed to wind a 7.27 μH primary is:

$$N = 31.5 (7.27/250) = 5.4$$

The primary/secondary turns ratio for this application is 1/1 so we also want a secondary winding with the same number of turns. The winding area, A_W , for each section of a two section bobbin, as indicated in the Winding Dimensions table, is 0.084 cm^2 .

$$T \geq N/A_W = 5.4/0.084 = 64$$

T is the minimum turns/cm² for the wire size that fits on the bobbin. The Magnet Wire Table indicates #18 wire (at 79.1 turns/cm²) or smaller. The resistance from the Wire table is 6.386 Ω /1000ft. and the average length per turn from the Winding Dimensions table is 0.121 feet, so the winding's resistance is:

$$R = N I_{WRW} = 5.4 \times 0.121 \times 6.386 = 0.0042\Omega$$

The average wire loss with a peak current of 7.15 Amps is then:

$$(I_{PK}^2 \times R)/3 = (7.15^2 \times 0.0042)/3 = 72\text{mW}$$

This is only 1.4% of the output power and should not be a problem. Our final transformer design is then:

- 1) 7.27 μH (about 10% tolerance) primary inductance
- 2) 1/1 primary/secondary turns ratio
- 3) 18 x 11 mm pot core with an A_L of 250 (example core: Magnetics Inc. #G-41811-25)

FERRITE POT CORE WINDING DIMENSIONS

Core Size (mm X mm)	Winding Area Per Section (cm ²)			Avg Length/Turn (Ft.)
	1 sect	2 sect	3 sect	
14 X 8	0.098	0.044	N/A	0.0953
18 X 11	0.170	0.084	0.049	0.121
22 X 13	0.292	0.138	0.087	0.145
26 X 16	0.421	0.202	0.128	0.173
30 X 19	0.542	0.254	0.159	0.204
36 X 22	0.755	0.357	0.225	0.244

AWG	HEAVY	QUAD	per in2	per cm2	Onms/1000	@750 Cir. mil/amp	@500 Cir. mil/amp
10	11,470	12,230	89	13.8	.9987	13,840	20,768
11	9,158	9,821	112	17.4	1.261	10,968	16,452
12	7,310	7,885	140	21.7	1.588	8,705	13,058
13	5,852	6,336	176	27.3	2.001	6,912	10,368
14	4,679	5,112	220	34.1	2.524	5,479	8,220
15	3,758	4,147	260	40.3	3.181	4,347	6,520
16	3,003	3,329	330	51.2	4.020	3,441	5,160
17	2,421	2,704	410	63.6	5.054	2,736	4,100
18	1,936	2,190	510	79.1	6.386	2,165	3,250
19	1,560	1,781	635	98.4	8,046	1,719	2,580
20	1,246	1,436	800	124	10.13	1,365	2,050
21	1,005	1,170	1,000	155	12.77	1,083	1,630
22	807	949	1,200	186	16.20	853	1,280
23	650	778	1,500	232	20.30	681	1,020
24	524	635	1,900	294	25.67	539	808
25	424	520	2,400	372	32.37	427	641
26	342	424	3,000	465	41.0	338	506
27	272	342	3,600	558	51.4	259	403
28	219	276	4,700	728	65.3	212	318
29	180	231	5,600	868	81.2	171	255
30	144	188	7,000	1,085	104	133	200
31	117	154	8,500	1,317	131	106	158
32	96.0	128	10,500	1,628	162	85	128
33	77.4	104	13,000	2,015	206	67	101
34	60.8	82.8	16,000	2,480	261	53	79
35	49.0	67.2	20,000	3,100	331	42	63
36	39.7	54.8	25,000	3,876	415	33	50
37	32.5	44.9	32,000	4,961	512	27	41
38	26.0	36.0	37,000	5,736	648	21	32
39	20.2	28.1	50,000	7,752	847	16	25
40	16.0	22.1	65,000	10,077	1,080	13	19
41	13.0		80,000	12,403	1,320	11	16
42	10.2		100,000	15,504	1,660	8.5	13
43	8.40		125,000	19,380	2,140	6.5	10
44	7.30		150,000	23,256	2,590	5.5	8
45	5.30		185,000	28,682	3,348	4.1	6.2

All the converter types referred to in this note are "fly-back" converters. They operate by charging an inductor from a DC input and then discharging the inductor to generate a DC output that is greater than, less than, or of opposite polarity to the input.

The proper inductor value for any DC-DC converter depends on three things: the desired output power, the input voltage (or range of input voltage), and the converter's oscillator frequency and duty cycle. This along with the input voltage, determine how much energy will be stored in the coil. The energy at a given instant is a function of the coil's current and inductance:

$$E_L = LI_{PK}^2/2$$

where

$$I_{PK} = V_L t_{ON}/L$$

The total power that can be put in (or taken out of) the coil is the energy (E_L) per cycle times the number of cycles per second.

$$P_L = E_L f_0$$

In the above equations, t_{ON} and f_0 are usually inter-dependent. Most often the clock is a 50% duty cycle square wave so:

$$t_{ON} = 1/(2f_0)$$

The coil power as a function of input voltage, frequency (duty cycle = 50%), and inductance is:

$$P_L = V_L^2/(8f_0 L), \text{ or in terms of } t_{ON}:$$

$$P_L = V_L^2 t_{ON}/(4L)$$

In step-up and inverting converters, the charging voltage for the coil (V_L) is usually the same as the input voltage (V_{IN}) if switch losses are ignored. In step-down converters, $V_L = V_{IN} - V_{OUT}$ (again ignoring losses) because the coil is connected between the input and output voltage when charging.

The above equations generally describe the design of MAX6XX DC-DC converter circuits. The following sections contain more specific design steps for each converter type.

Step-Up Regulator Design

(MAX630/631/632/633, MAX641/642/643)

First choose V_{OUT} , I_{OUT} , $V_{IN(min)}$, and $V_{IN(max)}$. Remember that in a step-up converter, V_{IN} must be less than V_{OUT} .

$V_{IN(min)}$, and $V_{IN(max)}$ cover the input voltage range, such as the beginning and end-of-life battery voltages. The output power P_{OUT} , is $V_{OUT} \times I_{OUT}$, but the converter also has to make up for losses in the inductor, L_x switch, and catch diode. These losses typically add 10 to 25% to the required power.

In a step-up converter, power is supplied both via the inductor and directly from the input voltage. This is be-

cause one end of the coil remains connected to V_{IN} as it supplies current to the output. Therefore:

$$1. P_{OUT} = P_L + V_{IN} I_{OUT}$$

The power, P_L , that we need from the inductor is then:

$$2. P_L = (V_{OUT} - V_{IN} + V_D) I_{OUT}$$

$V_D \times I_{OUT}$ accounts for losses in the catch diode. Schottky diodes (1N5817) minimize this loss which can be significant in low voltage circuits. In high voltage circuits ($V_{OUT} = 10V$ and up) or if efficiency is not critical, signal diodes such as 1N4148 perform well if their reverse voltage and forward current ratings are not exceeded.

In order to get P_L out of the inductor, that much power must be put in. In an ideal system, i.e., minimal switch losses, Eq. 3 or 4 provides the power in the coil:

$$3. P_L = V_L^2/(8f_0 L), \text{ or in terms of } t_{ON}:$$

$$4. P_L = V_L^2 t_{ON}/(4L)$$

Solving for the inductor value, L , and substituting Eq. 4 for P_L :

$$5. L = V_{IN(min)}^2 / 8f_0 I_{OUT} (V_{OUT} + V_D - V_{IN(min)})$$

f_0 is the DC-DC converter's clock frequency. Equation 5 assumes that f_0 is a square wave with a 50% duty cycle. On the MAX630 and MAX4193, the clock frequency can be adjusted. It is preset to a fixed rate (50kHz) on the MAX631/32/33 and cannot be changed. In Equation 5, the *minimum* expected value should be used for V_{IN} to insure that there is adequate output power under all input conditions.

In a non-ideal system, the inductor voltage, V_L , and the input voltage, V_{IN} , are not quite the same, largely because of switch ON resistance (R). The peak inductor current will not be the expected value if this resistance is significant. Instead of $I_{PK} = V_L t_{ON}/L$, the expression for inductor current changes to:

$$6. I_{PK} = V(1 - e^{-R t_{ON}/L})/R$$

The Expression for output power then changes to:

$$7. P_L = (V(1 - e^{-R t_{ON}/L})/R)^2 f_0 / 2$$

Besides inductance value, the selected coil must also be rated for the current that it must handle. The peak current that the coil sees is:

$$8. I_{PK} = V_{IN(max)} t_{ON}/L = V_{IN(max)}/2(f_0 L)$$

t_{ON} is the coil charging time (for one clock cycle) which is equivalent to one half of one f_0 clock period.

When calculating I_{PK} with Eq. 8, the largest expected value of V_{IN} ($V_{IN(max)}$) should be used so that the maximum current under all operating conditions will be considered. I_{PK} is then compared with the inductor current rating and the current rating of the L_x switch. I_{PK} should of course be less than these values.

If I_{PK} exceeds the peak current rating of the internal L_x switch in the MAX630/4193 (550mA) or

MAX631/632/633 (475mA) then an external MOSFET or transistor with an adequate current rating must be used. The MAX641/642/643 works best in most such circuits since they are designed to directly drive an external FET.

Step Down Regulator Design

(MAX638, and MAX631/32/33 driving P MOSFET)

Choose V_{OUT} , I_{OUT} , $V_{IN(min)}$, and $V_{IN(max)}$. In step-down converters, $V_{IN(min)}$ must be greater than V_{OUT} .

$V_{IN(min)}$ and $V_{IN(max)}$ define the converter's input voltage range, such as the unregulated power supply voltage at high and low power line voltages. Output power is $V_{OUT}I_{OUT}$, but the converter must also be able to supply power to make up for losses in the inductor, L_X switch, and catch diode. If an 80% conversion efficiency is assumed, P_{OUT} is multiplied by 1.25 in the equations below.

In a step-down converter such as the MAX638, the output power is the sum of the power supplied via the coil and the power supplied directly from the input voltage. When the coil charges, it is connected between the input and output so that inductor charging current also flows in to the load. When the coil discharges, current flows from ground, through the coil, into the load. Total output power is:

$$9. P_{OUT} = P_L + V_{OUT}I_{PK}/4$$

P_L is the power supplied by the coil and $V_{OUT}I_{PK}/4$ is the power supplied directly to the load while the coil charges. I_{PK} is the peak charging current of the inductor. The above equation assumes that the coil charging current rises linearly from 0 to I_{PK} during one half of each oscillator cycle. The average coil charging current is then $I_{PK}/4$.

$$10. I_{PK} = (V_{IN} - V_{OUT})t_{ON}/L$$

$$11. I_{PK} = (V_{IN(max)} - V_{OUT})/(2f_0L)$$

f_0 is the converter's clock frequency. The coil can charge for at most one half of each clock cycle ($1/2f_0$). By substituting Equation 11 into Equation 9, we get:

$$12. P_{OUT} = P_L + V_{OUT}(V_{OUT} - V_{IN})/(8f_0L)$$

In order to get P_L out of the inductor we must put at least that much in. The power that is put in is:

$$13. P_L = (V_{IN} - V_{OUT})^2/(8f_0L)$$

By substituting Equation 13 into Equation 12, we get:

$$14. P_{OUT} = V_{IN}(V_{IN} - V_{OUT})/(8f_0L)$$

In terms of L , and by multiplying P_{OUT} by 1.25 to account for typical losses, we get:

$$15. L = V_{IN(min)}(V_{IN(min)} - V_{OUT})/(10f_0P_0)$$

The minimum expected value should be used for V_{IN} to ensure that there is adequate power under all conditions.

Besides inductance value, the selected coil must also be rated for the current that it will be handling in the circuit. The peak coil current is expressed by Equation 11. When calculating I_{PK} , $V_{IN(max)}$ should be used so that the maximum current under all operating conditions will be considered. I_{PK} is then compared with the current ratings of the inductor and L_X switch, and must be less than these values.

If I_{PK} exceeds the peak current rating of the internal L_X switch in the MAX638 (550mA) an external MOSFET or transistor, that is rated for the current, can be used with a MAX631/2/3 converter. Although they are called "step-up" regulators they can easily be configured for step-down circuits when using an external MOSFET. The MAX638 may also be used with an external transistor, but an inverter is also required.

Inverting Regulator Design

(MAX634/635/636)

Choose V_{OUT} , I_{OUT} , $V_{IN(min)}$ and $V_{IN(max)}$. In an inverting DC-DC converter, V_{IN} may be greater, equal, or less than V_{OUT} .

Output power is $V_{OUT}I_{OUT}$, but the converter has to supply additional power to make up for losses. These typically add 10 to 25% to the required power, depending on external conditions such as component selection and operating voltage. If we assume a conversion efficiency of 80%, the required power is multiplied by 1.25 in the initial design.

In an inverting converter (MAX634/5/6/7), all output power is supplied via the coil. One end of the coil remains grounded when it charges and discharges. The total output power is:

$$16. P_{OUT} = P_L$$

P_L is the power supplied by the coil. In order to get P_L out of the inductor, P_L must be put in:

$$17. P_L = V_{IN}^2/(8f_0L)$$

Solving for the inductor value and assuming 80% efficiency:

$$18. L = V_{IN(min)}^2/(10f_0I_{OUT}V_{OUT})$$

f_0 is the DC-DC converter's clock frequency and assumes that f_0 is a square wave with a 50% duty cycle. On the MAX634, the clock can be adjusted while the MAX635/6/7 has a preset oscillator that cannot be changed. In Equation 18, $V_{IN(min)}$ should be used to ensure that there is adequate power under all conditions.

Besides inductance value, the selected coil must also be rated for the current it must handle. The peak current that the coil sees is:

$$19. I_{PK} = V_{IN(max)}t_{ON}/L = V_{IN(max)}/(2f_0L)$$

t_{ON} is the coil charging time (for one clock cycle) which is equivalent to one half of one f_0 clock period.

When calculating I_{PK} with Equation 19, the largest expected value of V_{IN} ($V_{IN(max)}$) should be used so that the maximum current under all operating conditions is considered. I_{PK} is then compared with the inductor current rating and the current rating of the L_X switch. I_{PK} should of course be less than these values. If I_{PK} exceeds the peak current rating of the internal L_X switch in the MAX634 (550mA) or MAX635/6/7 (475mA), an external MOSFET or transistor with an adequate current rating must be used.

Transformer DC-DC Converter Design

In designs which employ flyback transformers, step-up, step-down, or inverting converters are all built using the same basic architecture. As with other DC-DC designs, first choose V_{OUT} , I_{OUT} , $V_{IN(min)}$, and $V_{IN(max)}$. Remember that although the power to the load is $V_{OUT}I_{OUT}$, the converter has to supply 10% to 25% more power to make up for diode, switch and transformer losses. In flyback transformer circuits, all output power is supplied via the transformer so:

$$20. P_{OUT} = P_T - V_{DOUT}$$

P_T is the power supplied via the transformer and V_{DOUT} is the power lost in the steering diode. In order to get P_T out of the transformer secondary, P_T must be put into the primary.

$$21. P_T = V_{IN}^2 / (8f_0 L_{PRI})$$

Solving for the transformer's primary inductance:

$$22. L_{PRI} = V_{IN(min)}^2 / (8f_0 I_{OUT}(V_{OUT} + V_D))$$

f_0 is the DC-DC converter's clock frequency and assumes that f_0 is a square wave with a 50% duty cycle. The MAX634 and MAX630 allow the clock frequency to be adjusted while other devices have a preset oscillator (typically 50kHz) that cannot be changed. In Equation 22, $V_{IN(min)}$ should be used for V_{IN} to insure that there is adequate power under all input conditions.

Besides inductance value, the transformer must also be rated for the proper peak current. The peak current is:

$$23. I_{PK} = V_{IN(max)} I_{ON} / L_{PRI} = V_{IN(max)} / (2f_0 L)$$

I_{ON} is the charging time (for one clock cycle) which is equivalent to one half of one f_0 clock period.

When calculating I_{PK} with Equation 23, the largest expected value of $V_{IN}(V_{IN(max)})$ should be used so that the maximum current under all operating conditions will be considered. I_{PK} is then checked against MAX6XX's L_X switch current rating and also determines the current handling requirements of the transformer. L_{PRI} and I_{PK} are then used for transformer design.

Benchmark Shortcut

The most direct means of checking I_{PK} is to measure it using an oscilloscope and current probe. If a current probe is not available, a less direct but still effective method is to observe the current by looking differentially across a small sense resistor placed in series with the inductor. 1 Ω usually does well, but a smaller value is necessary if currents over a few hundred milliamps are expected.

The following is a partial listing of sources for inductors, transformers, and cores for DC-DC converter magnetic components. It is by no means intended as a complete list.

AIE Magnetics
701 Murfreesboro Rd.
Nashville, TN 37210
TEL 615-244-9024

AIE makes a variety of coils and transformers. Their full line catalog lists a variety of inductors. Catalog 5 lists many transformers designed for flyback converters up to 50watts. Catalog 3 lists many coil types: slugs, toroids, pot cores, etc.

BH Electronics
12219 Wood Lake Dr.
Burnsville, MN 55337
TEL 612-894-9590
FAX 612-894-9380

Coils and transformers from miniature surface mount up through 10's of watts.

Caddell-Burns
40 East Second Street
Mineola, NY 11501
TEL 516-746-2310

Caddell-Burns has many standard coils in their 6860 and 70790 series which are suitable for use with Maxim's DC-DC converters. 7070 series coils have high current ratings for their size. Efficiencies that match toroids can be achieved.

Dale Electronics
East Highway 50
Yankton, SD 57078
TEL 605-665-9301

Standard toroidal inductors in molded PC mount packaging.

Gowanda Electronics
1 Industrial Place
Gowanda, NY 14070
TEL 716-532-2234

Gowanda makes coils ranging from surface mount devices up through high power toroids, and also has many inductors wound on cylindrical ferrite bobbins. They make transformers in port cores, E cores, and Toroids.

Inductor Supply
1849 West Sequoia Ave.
Orange, CA 92668-1017
TEL 714-978-2277
FAX 714-978-2411

Inductor Supply is a low-cost supplier of bobbin, shielded, and molded inductors. They also make surface mount inductors and custom magnetics.

J.W. Miller
19070 Reyes Ave.
PO Box 5825
Rancho Dominguez,
CA 90224
TEL 213-537-5200
FAX 213-631-4217

Miller has standard coils and toroids at low cost, however, avoid the tiny moulded cokes. The series resistance and current ratings of the small moulded parts are generally not adequate for DC-DC applications except in extremely low power applications (mA).

National Electronics
11731 Markon Drive
Garden Grove, CA 92641
TEL 714-892-7749
FAX 714-898-6769

In Addition to manufacturing their own line of low-cost bobbin, drum, and toroid inductors, National distributes TDK, Jeffers, Delevan, and Nytronics products.

Nytronics Components
Group, Inc.
Orange Street
Darlington, SC 29532
TEL 803-393-5421

Small molded inductors which generally do not have adequate current capability for DC-DC circuits except in very low current applications (mA).

Pulse Engineering
PO Box 12235
San Diego, CA 92112
TEL 619-268-2400
FAX 619-268-2515

Pulse Eng. supplies a line of low cost toroids, as well as mounted and molded toroids. A toroid sampler kit, #845, is useful for prototyping designs. Custom transformers are also available.

Prem Magnetics
3521 N. Chapel Hill Rd.
McHenry, IL 60050
TEL 815-642-3763
TWX 910-642-3763

Renco Electronics
60 Jefferson Blvd E.
Deer Park, NY 11729
TEL 516-586-5566
FAX 516-586-5562

Renco has a broad line of of bobbin and molded standard coils. Custom transformers and toroids are also supplied.

Schott Corporation
Suite 108
1838 Elm Hill Pike
Nashville, TN 37210
TEL 615-889-8800
FAX 612-885-0834

Schott makes both miniature toroids, pot core inductors and transformers. Custom designs are available.

Torotel Products Inc.
13402 S. 71 Highway
Grandview, MO 64030
TEL 816-761-6314
TWX 910-777-7037

Torotel specializes in toroidal inductors. Their general catalog lists hundreds of sizes and inductances. Mil Spec versions are available

Wilco Corporation
6451 Saguaro Court
Indianapolis, IN 46268
TEL 317-293-9300
FAX 317-293-9462

Wilco makes small high current coils as well as other fixed inductors. Toroidal inductors are also sold.

Manufacturer - Asia
TDK Corporation
13-1, Nihonbashi 1-chome
Chuo-ku
Tokyo 103 Japan

Manufacturer - Europe
Richard Jahre GmbH
Luetzowstrasse 90
1000 Berlin 30

Allen-Bradley Magnetic Products
5900 N. Harrison Street
Shawnee, OK 74801
TEL 405-275-2100
TLX 796208

Arnold Engineering Company
300 West Street
Marengo, IL 60152
TEL 815-568-2000
TWX 910-642-2790

Fair-Rite
P.O. Box J
1 Commercial Row
Wallkill, NY 12589
TEL 914-895-2055
FAX 914-895-2629

Ferronics
45 O'Connor Road
Fairport, NY 14450
TEL 716-388-1020
FAX 716-388-0036

Ferroxcube
5083 Kings Highway
Saugerties, NY 12477
TEL 914-246-2811
TWX 510-247-5410

Magnetics
Div of Spang and Co.
900 E. Butler Rd.
PO Box 391
Butler, PA 16003
TEL 412-282-8282
TWX 710-373-3821

Publication MPCC contains information on both soft/linear ferrite and permanent magnetics. The key section is the "W5" section which provides info on their optimum material for DC-DC converters, as well as pot cores and toroids made from this material.

Arnold makes cores in both iron powder and molypermalloy powder (MPP).

Fair-Rite makes forms for a variety of bobbins, beads, and cores. Their technical literature contains information on ferrite manufacturing technology as well inductor design.

Ferronics makes bobbin and toroid ferrite cores plus ferrite beads and magnets. Their literature contains some good technical information on inductor design.

Ferroxcube's Linear Ferrite Materials and Components catalog lists a wide variety of cores: toroids, pot cores, square cores, EP, EC, etc. The catalog has complete data on the cores and material, but little applications information.

Magnetics has a complete line of magnetic materials: The ferrites and MPP cores are the most useful for DC-DC converters. A complete catalog/binder with both inductor design information and complete product data is available. All of the standard core shapes are available: pot cores, EE, EI, bobbin, toroids, etc. The catalog contains useful coil design information.

Micrometals, Inc.
1190 N. Hawk Circle
Anaheim, CA 92807
TEL 714-630-7420
TWX 910-591-1690

Siemens Components Inc.
Special Products Division
186 Wood Avenue South
Iselin, NJ 08830
TEL 201-321-3400

Permag Inc.,
Regional offices

Atlanta	404-448-4998
Boston	617-273-2890
Chicago	312-956-1140
Dallas	214-699-1121
Colorado	303-693-6612
Los Angeles	714-952-2091
Minneapolis	612-934-4635
San Francisco	408-738-1080
Toledo	419-385-4621
NY/LI	516-822-3311

Cores Unlimited, Inc.
8311 Westminster Ave
Suite 340F
Westminster, CA 92683
TEL 714-894-3062
800-772-core
FAX 714-895-4502

Low cost iron powder cores in toroids, E cores, and bars. These are lower cost than MPP or ferrite, but have lower efficiency.

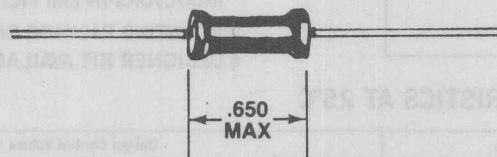
The "Ferrite Cores and Hardware" short form catalog provides information on pot cores from 3.3x2.6mm to 41x25mm; toroids from 2.5mm to 34mm diameter, and a wide variety of other shapes such as E and RM.

Permag is a Distributor of Magnetic Cores for Allen-Bradley, Stackpole, Siemens, and Krystinel.

Cores Unlimited is an authorized distributor of magnetic cores for Hitachi and Siemens. They also handle cores from several other manufacturers.

"SFB" SERIES • SMALL FERRITE Bobbin Coils

- Leads No. 20 Tinned Copper 1.5" long
- Coils Finished with Polyolefin Shrink Tube
- Nonstandard Values Available
- Saturation Current Lowers Inductance 5%



WILCO PART #	L uh ± 15%	R.D.C. OHMS MAX.	Saturation Current (DC AMPS)	I AMPS Suggested Rating	DIA. NOM.	TEST FREQ.
SFB 39G	3.9	.019	7.3	1.28	.260	1 KHz
SFB 47G	4.7	.022	6.3	1.28	.260	1 KHz
SFB 56G	5.6	.024	5.6	1.28	.260	1 KHz
SFB 68G	6.8	.026	5.3	1.28	.260	1 KHz
SFB 82G	8.2	.028	4.5	1.28	.260	1 KHz
SFB 100	10	.033	4.1	1.28	.260	1 KHz
SFB 120	12	.037	3.6	1.28	.260	1 KHz
SFB 150	15	.040	3.3	1.28	.260	1 KHz
SFB 180	18	.044	3.0	1.28	.260	1 KHz
SFB 220	22	.050	2.7	1.28	.260	1 KHz
SFB 270	27	.058	2.5	1.28	.260	1 KHz
SFB 330	33	.075	2.2	1.008	.260	1 KHz
SFB 390	39	.094	2.0	.804	.260	1 KHz
SFB 470	47	.109	1.8	.804	.260	1 KHz
SFB 560	56	.140	1.7	.804	.260	1 KHz
SFB 680	68	.131	1.5	.804	.260	1 KHz
SFB 820	82	.152	1.4	.804	.260	1 KHz
SFB 101	100	.208	1.2	.632	.260	1 KHz
SFB 121	120	.283	1.1	.508	.260	1 KHz
SFB 151	150	.340	1.0	.508	.260	1 KHz
SFB 181	180	.362	.95	.508	.260	1 KHz
SFB 221	220	.430	.86	.508	.260	1 KHz
SFB 271	270	.557	.77	.400	.260	1 KHz

WILCO PART #	L uh ± 15%	R.D.C. OHMS MAX.	Saturation Current (DC AMPS)	I AMPS Suggested Rating	DIA. NOM.	TEST FREQ.
SFB 331	330	.665	.70	.400	.260	1 KHz
SFB 391	390	.712	.64	.400	.260	1 KHz
SFB 471	470	1.15	.59	.315	.260	1 KHz
SFB 561	560	1.27	.54	.315	.260	1 KHz
SFB 681	680	1.61	.49	.250	.260	1 KHz
SFB 821	820	1.96	.44	.200	.260	1 KHz
SFB 102	1000	2.30	.40	.200	.260	1 KHz
SFB 122	1200	2.65	.35	.200	.260	1 KHz
SFB 152	1500	3.45	.33	.158	.260	1 KHz
SFB 182	1800	4.03	.29	.158	.260	1 KHz
SFB 222	2200	4.48	.27	.158	.260	1 KHz
SFB 272	2700	5.40	.24	.125	.260	1 KHz
SFB 332	3300	6.56	.22	.125	.260	1 KHz
SFB 392	3900	8.63	.20	.100	.260	1 KHz
SFB 472	4700	9.66	.18	.100	.260	1 KHz
SFB 562	5600	13.9	.166	.082	.260	1 KHz
SFB 682	6800	16.3	.151	.082	.260	1 KHz
SFB 822	8200	20.8	.138	.065	.260	1 KHz
SFB 103	10000	26.4	.125	.050	.260	1 KHz
SFB 123	12000	29.9	.114	.050	.260	1 KHz
SFB 153	15000	42.5	.098	.039	.260	1 KHz
SFB 183	18000	48.3	.091	.039	.260	1 KHz

WILCO CORPORATION

6451 SAGUARO COURT

317-293-9300

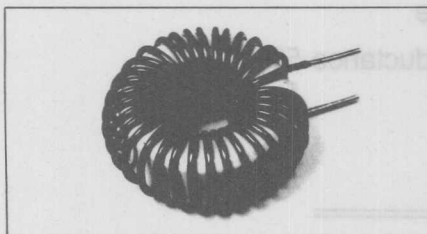
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LOWEST COST INDUCTORS

NEW

ELECTRICAL DATA



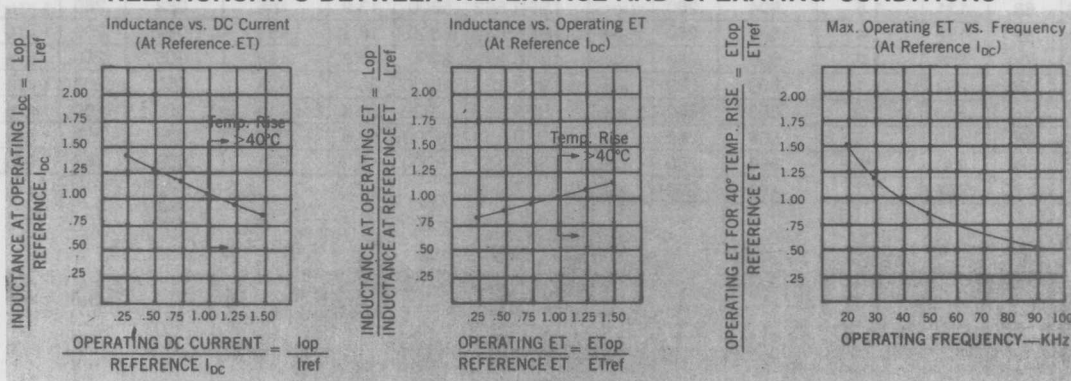
- SMPS AVERAGING FILTER (4)
- CHARACTERIZED FOR GENERAL PURPOSE USE, AND RIPPLE FILTERS
- SINGLE LAYER DESIGNS
- CAN BE USED AS DIFFERENTIAL MODE INDUCTORS IN EMI FILTERS (3)
- MOUNTING PACKAGE AVAILABLE ON REQUEST
- DESIGNER KIT AVAILABLE

ELECTRICAL CHARACTERISTICS AT 25°C

Reference Operating Values					Design Control Values (2)						
Part Number	Klip Mount Option	Inductance Typical (μ Hy) ⁽¹⁾	I _{DC} (AMPS)	ET _{OP} (V- μ Sec)	Inductance No D.C. +20% (μ Hy) -12%	1000 Hz Test Volts No D.C.	D C R (OHMS) Max	Coil Size Code	Klip Mount Package	Lead Dia. (In) ^{±.003}	Min. Energy Storage (μ J) ⁽⁵⁾
51591		20	2.0	52	32.8	.0034	.06	H		.020	40
92100	K	25	2.5	30	20.7	.0023	.04	A	KM1	.020	75
92101	K	50	2.5	50	45.7	.0047	.07	B	KM2	.020	150
92102	K	100	2.5	90	94.1	.0094	.10	C	KM3	.020	300
92103	K	35	2.5	55	28.4	.0037	.04	B	KM2	.025	110
92104	K	70	3.0	85	61.0	.0076	.05	C	KM3	.025	300
92105	K	145	3.0	140	141.8	.015	.08	D	KM4	.025	650
92106	K	285	3.0	300	264.1	.035	.14	E	KM5	.025	1275
92107		450	3.0	425	436.3	.053	.20	F		.025	2000
92108	K	100	3.5	130	90.7	.012	.04	D	KM4	.032	600
92109	K	165	4.0	240	152.0	.027	.07	E	KM5	.032	1300
92110		270	4.0	350	263.9	.041	.10	F		.032	2150
92111	K	40	4.0	70	37.9	.006	.03	C	KM3	.032	300
51590		12	5.0	44	20.3	.0038	.03	G		.032	150
92112	K	100	5.0	200	90.7	.021	.04	E	KM5	.042	1250
92113		170	5.0	300	159.7	.032	.05	F		.042	2100
92114	K	55	5.0	100	54.9	.009	.02	D	KM4	.042	650
92115		95	7.0	225	96.0	.025	.03	F		.051	2300
92116	K	55	7.0	150	49.1	.015	.02	E	KM5	.051	1300
92117		55	10.0	175	55.9	.019	.02	F		.064	2750

See page 5 for Notes

RELATIONSHIPS BETWEEN REFERENCE AND OPERATING CONDITIONS



Pulse Engineering

P.O. BOX 12235 SAN DIEGO, CA 92112 619-268-2400

QUALITY COILS SINCE 1946



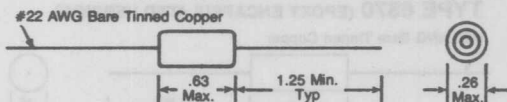
258 East Second Street
Mineola, New York 11501-3508

Area Code 516 746-2310

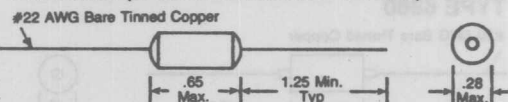
MINIATURE HIGH CURRENT CHOKES

1.0 μ H - 100mH. 10% Tolerance. Recommended Mounting Pitch — .80"

TYPE 7070



TYPE 7080 (EPOXY ENCAPSULATED VERSION)



NOTES: (FOR BOTH TYPES)

1. INDUCTANCE:

For 1.0 μ H thru 8.2 μ H; effective inductance measured on Boonton 260A Q-meter at 7.9 MHz in accordance with MIL-C-15305.
For 10 μ H thru 100mH; inductance (Ls) measured on General Radio 1650B Impedance Bridge at 1 KHz.

2. Current rating (Rated IDC) is based on 0.25 watt power dissipation for approximately 20°C temperature rise. Depending on the application, these units may be operated at up to twice the rated current.

3. Incremental current (INCR I) is the minimum current at which the inductance will be decreased by 5% from its initial (zero-DC) value.

4. Dielectric Withstanding Voltage — 1000 VRMS.

5. Operating temperature range — 55° to +105°C.

6. Materials:

Coil Form: Ferrite

Cover: TYPE 7070 - PVC shrink tube-flame retardant UL type

FR-1 per MIL-I-23053

TYPE 7080 - Epoxy encapsulated.

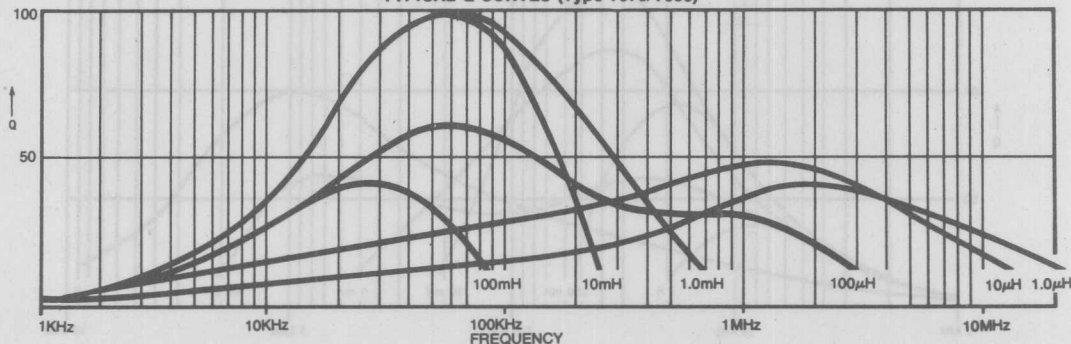
Magnet Wire: Per FED SPEC J-W-001177/9 (MIL-W-583 Type B)

STANDARD VALUES: (Electrical characteristics are identical for both types. Other values are available on special order.)

DASH NO.	NOMINAL INDUCTANCE	MAX.DCR OHMS	MIN.SRF μ H	RATED IDC ma	INCR I ma
-01	1.0 μ H	.010	155	5,000	6,400
-02	1.2	.011	148	4,800	6,000
-03	1.5	.012	128	4,800	5,000
-04	1.8	.013	120	4,400	4,500
-05	2.2	.014	108	4,200	4,100
-06	2.7	.015	100	4,100	3,600
-07	3.3	.016	96	4,000	3,200
-08	3.9	.017	90	3,800	3,000
-09	4.7	.022	85	3,400	2,700
-10	5.6	.028	76	3,000	2,500
-11	6.8	.031	70	2,800	2,300
-12	8.2	.035	51	2,700	2,000
-13	10	.038	35	2,600	1,900
-14	12	.043	21	2,400	1,700
-15	15	.049	14	2,300	1,500
-16	18	.054	10	2,200	1,400
-17	22	.059	8.0	2,100	1,300
-18	27	.070	6.5	1,900	1,100
-19	33	.077	6.1	1,800	1,000
-20	39	.084	5.7	1,700	940
-21	47	.093	5.1	1,600	870
-22	56	.12	4.3	1,500	790
-23	68	.13	3.6	1,400	710
-24	82	.16	3.2	1,300	650
-25	100	.24	3.0	1,000	590
-26	120	.32	2.7	880	540
-27	150	.43	2.1	760	480
-28	180	.48	1.7	720	440
-29	220	.55	1.6	670	400
-30	270	.62	1.5	640	360

DASH NO.	NOMINAL INDUCTANCE	MAX.DCR OHMS	MIN.SRF μ H	RATED IDC ma	INCR I ma
-31	330 μ H	.72	1.4	590	320
-32	390	.79	1.3	560	300
-33	470	.88	1.2	530	270
-34	560	1.2	1.1	460	250
-35	680	1.5	1.0	410	230
-36	820	1.7	.96	380	210
-37	1.0mH	1.9	.88	360	190
-38	1.2	2.4	.78	320	170
-39	1.5	2.8	.64	300	150
-40	1.8	3.1	.60	280	140
-41	2.2	4.5	.54	240	120
-42	2.7	5.8	.44	210	110
-43	3.3	8.1	.43	180	100
-44	3.9	8.9	.40	170	95
-45	4.7	10	.38	160	86
-46	5.6	11	.35	150	79
-47	6.8	15	.29	130	72
-48	8.2	17	.26	120	65
-49	10	22	.24	110	59
-50	12	26	.23	100	54
-51	15	34	.19	86	48
-52	18	39	.17	80	44
-53	22	54	.16	68	40
-54	27	62	.15	64	36
-55	33	82	.12	55	32
-56	39	93	.11	52	30
-57	47	120	.096	46	27
-58	56	130	.092	44	25
-59	68	190	.088	36	23
-60	82	210	.080	35	21
-61	100	270	.074	30	19

TYPICAL Q CURVES (Type 7070/7080)



QUALITY COILS SINCE 1946



258 East Second Street
Mineola, New York 11501-3508

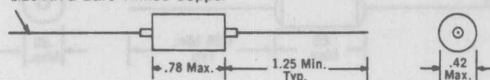
Area Code 516 746-2310

HIGH CURRENT CHOKES

10 μ H-1.0H. 10% Tolerance. Recommended Mounting Pitch — 1.25"

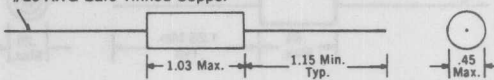
TYPE 6860

#20 AWG Bare Tinned Copper



TYPE 6870 (EPOXY ENCAPSULATED VERSION)

#20 AWG Bare Tinned Copper



NOTES: (FOR BOTH TYPES)

- Inductance (Ls) measured on General Radio 1650B Impedance Bridge at 1 KHz.
- Current rating (Rated IDC) is based on 0.5 watt power dissipation for approximately 20°C temperature rise. Depending on the application, these units may be operated at up to twice the rated current.
- Incremental current (INCR I) is the minimum current at which the inductance will be decreased by 5% from its initial (zero-DC) value.

4. Dielectric Withstanding Voltage — 1000 VRMS.

5. Operating temperature range — 55° to + 105°C.

6. Materials:

Coil Form: Ferrite.

Cover: TYPE 6860 - Polyester alpha-cellulose.

Coating: Polyurethane per MIL-1-46058.

TYPE 6870- Cover & Coating: Epoxy encapsulated.

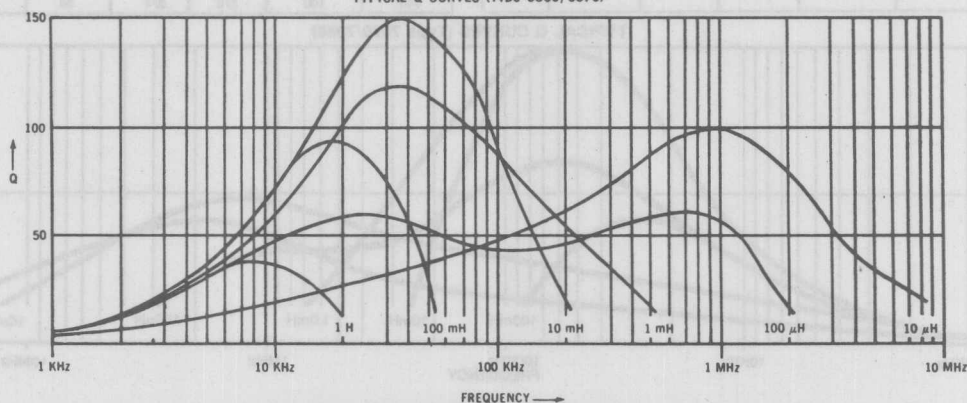
Magnet Wire: Per FED SPEC J-W-001177/9 (MIL-W-583 Type B)

STANDARD VALUES: (Electrical characteristics are identical for both types. Other values are available on special order.)

Dash No.	Nominal Inductance	Max. DCR Ohms	Min. SRF MHz	Rated IDC ma	INCR I ms
-01	10 μ H	.023	.45	4600	3200
-02	12	.025	.40	4500	2900
-03	15	.030	.32	4100	2600
-04	18	.032	.21	3900	2400
-05	22	.035	.12	3700	2200
-06	27	.038	.85	3600	2000
-07	33	.043	.58	3400	1800
-08	39	.047	.35	3200	1700
-09	47	.054	.32	3000	1500
-10	56	.060	.29	2900	1400
-11	68	.068	.27	2700	1200
-12	82	.073	.25	2600	1100
-13	100	.098	.23	2300	1000
-14	120	.14	.21	1900	930
-15	150	.18	.19	1700	830
-16	180	.20	.15	1600	760
-17	220	.28	.13	1400	680
-18	270	.31	.13	1300	620
-19	330	.35	.12	1200	560
-20	390	.38	.11	1100	510
-21	470	.44	.10	1050	460
-22	560	.48	.90	1000	430
-23	680	.63	.80	890	390
-24	820	.87	.72	760	350
-25	1.0 mH	.96	.65	720	320
-26	1.2	1.3	.62	620	290
-27	1.5	1.4	.58	600	260
-28	1.8	1.7	.53	540	240
-29	2.2	2.3	.44	470	220
-30	2.7	2.6	.39	440	190
-31	3.3	3.5	.36	380	160

Dash No.	Nominal Inductance	Max. DCR Ohms	Min. SRF MHz	Rated IDC ma	INCR I ms
-32	3.9 mH	3.8	.34	360	160
-33	4.7	4.3	.32	340	150
-34	5.6	5.6	.26	300	140
-35	6.8	6.3	.24	280	120
-36	8.2	8.6	.21	240	110
-37	10	9.7	.20	220	100
-38	12	11	.19	210	92
-39	15	15	.17	180	84
-40	18	20	.14	160	75
-41	22	24	.13	140	68
-42	27	26	.12	130	62
-43	33	35	.10	120	56
-44	39	38	.95	110	51
-45	47	50	.80	100	47
-46	56	55	.72	95	43
-47	68	76	.66	81	39
-48	82	86	.62	76	35
-49	100	99	.57	71	32
-50	120	110	.52	67	29
-51	150	200	.47	50	26
-52	180	220	.43	48	24
-53	220	300	.38	41	22
-54	270	320	.35	40	20
-55	330	420	.32	35	18
-56	390	480	.29	32	16
-57	470	670	.26	27	15
-58	560	730	.24	26	14
-59	680	870	.19	24	12
-60	820	950	.18	23	11
-61	1.0 H	1100	.17	21	10

TYPICAL Q CURVES (Type 6860/6870)



Representative Power MOSFETs

Part Number	PACKAGE	R _{ON} (@) at (I _{DS} , V _{GS} = xV)	Volts (max)	Mfg**
N Channel				
BUZ71A	TO-220	0.12 (6A, V _{GS} = 10V)	50	MOT/SI/SM
BUZ21	TO-220	0.1 (9A, V _{GS} = 10V) 0.2 (5A, V _{GS} = 5V)*	100	MOT/SI/SM
IRF513	TO-220	0.8 (2A, V _{GS} = 10V) 1.2 (1A, V _{GS} = 5V)*	100	IR/SI/GE/MOT
IRF530	TO-220	0.18 (8A, V _{GS} = 10V) 2.0 (4A, V _{GS} = 5V)*	100	IR/SI/GE/MOT
IRF540	TO-220	0.085 (8A, V _{GS} = 10V) 0.1 (5A, V _{GS} = 5V)*	100	IR/SI/GE/MOT
IRF620	TO-220	0.8 (2.5A, V _{GS} = 10V) 1.3 (2.5A, V _{GS} = 5V)*	200	IR/SI/GE/MOT
IRF640	TO-220	0.18 (10A, V _{GS} = 10V)	200	IR/SI/GE/MOT
IRFD121	4p DIP	0.3 (1.3A, V _{GS} = 10V)	60	IR/GE
RFP12N08L	TO-220	0.2 (1.3A, V _{GS} = 5V)	80	RCA
P Channel				
IRFD9120	4p DIP	0.6 (1.3A, V _{GS} = -10V)	-100	IR/GE
IRF9520	TO-220	0.6 (3.5A, V _{GS} = -10V)	-100	IR
IRF9540	TO-220	0.2 (10A, V _{GS} = -10V)	-100	IR
IRF9543	TO-220	0.3 (10A, V _{GS} = -10V)	-60	IR
IRF9620	TO-220	1.5 (3.5A, V _{GS} = -10V)	-200	IR
RFP6P08	TO-220	0.6 (V _{GS} = -10V)	-100	RCA
MTP2P45	TO-220	6 (1A, V _{GS} = -10V)	-450	MOT
MTP8P08	TO-220	0.4 (4A, V _{GS} = -10V)	-80	MOT

* Typical specification, not guaranteed by manufacturer.

** Manufacturer code: IR = International Rectifier, SI = Siliconix, MOT = Motorola, GE = General Electric, SM = Siemens, RCA = RCA

Rectifiers for DC-DC Converter Circuits

Part Number	I _{AVG} (amps)	V _F (Volts)	PRV (VOLTS)	Type	PACKAGE
1N914	0.05	1.0	75	Silicon	Glass
1N4148	0.05	1.0	75	Silicon	Glass
1N4935	1	1.2	200	Silicon	Plastic
1N5817	1	0.45	20	Schottky	Plastic
1N5818	1	0.55	30	Schottky	Plastic
1N5820	3	0.475	20	Schottky	Plastic
1N5821	3	0.5	30	Schottky	Plastic
1N5822	3	0.525	40	Schottky	Plastic
1N5823	5	0.36	20	Schottky	Metal
1N5824	5	0.37	30	Schottky	Metal
1N5825	5	0.38	40	Schottky	Metal
UDS620	6	0.48	20	Schottky	TO-220
UDS640	6	0.48	40	Schottky	TO-220
UES1001	1	0.895	50	Silicon	Bead
UES1002	1	0.895	100	Silicon	Bead
UES1003	1	0.895	150	Silicon	Bead

Primary Batteries

Dry Cells

There are three popular cell types based on zinc and carbon: the standard LeClanche dry cell, the "heavy duty" zinc chloride cell, and the alkaline manganese cell. As shown in Table 1, there is about a 3 to 1 difference in capacity between the alkaline and LeClanche at the 100 hour discharge rate. The zinc chloride battery falls about midway between the other two. The most significant difference between the characteristics of these three chemistries is their response to high load currents, and their response to continuous versus pulsed applications.

In very low drain applications such as 1mA from a D cell, the LeClanche cell has about 1/2 the capacity of the alkaline (7Ah vs. 16Ah). When the load current is increased to 80mA, the duty cycle begins to play an important role. The alkaline battery loses virtually no capacity when operated continuously at 80mA, but the LeClanche cell capacity drops from 4Ah to 2.3Ah as the duty cycle of the 80mA load is increased from 1h/day to 24h/day. The zinc chloride cell has 6.2 Ah and 6.0Ah capacity under 80mA load, 1h/day and 24h/day respectively.

Summary: The alkaline cell has about twice the capacity of a LeClanche under very light loads and is over 6 times better under continuous duty high current loads.

Mercury

This cell has a very stable output voltage of about 1.35V, except for those cells which have a small amount of manganese dioxide added, which raises the open circuit volt-

age to 1.4V. It has good storage characteristics, retaining 85% to 90% capacity after two years at 20°C, and about 80% after one year of storage at 45°C. Mercury cells are generally not recommended for use below 0°C. The "9V" size 6 cell mercury battery has an output voltage of 7.5 to 8.0V for virtually all of its life, and has about 575mAh capacity. The capacity of mercury batteries is nearly independent of duty cycle, except at very high discharge rates. It is generally more expensive than alkaline cells, which have nearly the same performance, except that the output voltage of alkaline cells changes more as the cell is discharged.

Silver Oxide

Primarily used for miniature button and coin cells such as those used in watches and hearing aids, the silver oxide cell has a flat 1.55V discharge. They are best for light loads of C/50 or less. It retains about 70% of its capacity when operated at 0°C, and about 30% at -20°C.

Lithium Manganese Dioxide (LiMnO₂)

There are two basic types of LiMnO₂ cells. A pressed powder cathode is used in low discharge rate cells such as the "coin" cells. Flat and cylindrical cells with higher discharge current ratings use a thin electrode pasted on a supporting grid structure. The open circuit voltage is slightly higher than 3.0V. The output voltage is relatively flat at 2.8V to 3.0V up to the last 20% of the discharge period. Like most lithium chemistries, LiMnO₂ cells have very good storage characteristics, with about 85% of capacity remaining after 6 years storage at 20°C.

Performance of Primary (Non-Rechargeable) Batteries

Chemistry Anode/Cathode/Electrolyte	Open Circuit V	Loaded V	Capacity (Ah at 100 hr rate)	Energy (Watts - hr)	Weight (grams)	Energy Density	
						Wh/kg	Wh/Liter
Alkaline Zn/MnO ₂ /KOH	1.58	1.5-1.1	14	17	132	125	315
Carbon Zinc (LeClanche) Zn/MnO ₂ /NH ₄ CL,ZnCl ₂	1.55	1.5-1.0	4.5	5.4	95	55	100
Mercury Zn/HgO/KOH	1.35	1.3	15	18	166	100	450
Lithium Sulfur Dioxide Li/SO ₂ /LiBr	3.0	2.8-2.7	8	22	95	275	440
Lithium Thionyl Chloride Li/SOCl ₂ /LiAlCl ₄	3.9	3.9-3.5	14	45	113	375	850
*Lithium poly-carbonmonofluoride nLi/(CF) _n / -butyrolactone	3.0	2.6	10	26	94	275	500
*Lithium Manganese Dioxide Li/MnO ₂	3.25	3.0-2.0	14	26	130	230	500

*Extrapolated from data for smaller cells.

Performance of Secondary (Rechargeable) Batteries

Chemistry Anode/Cathode/Electrolyte	Open Circuit V	Loaded V	Capacity (Ah at 100 hr rate)	Energy (Watts - hr)	Weight (grams)	Energy Density	
						Wh/kg	Wh/Liter
Nickel Cadmium Ni/Cd/KOH	1.35	1.25	4.4	5.3	140	40	120
Lead Acid PbO ₂ /Pb/H ₂ SO ₄	2.1	2.0	2.7	5.4	182	30	100

This is the most mature of the high energy density, high discharge rate lithium chemistries and has been extensively used in military applications such as sonobuoys, radios, and beacons. Early LiSO_2 had some safety problems, but manufacturers now extensively test their designs. Indeed, many data sheets have more information about crush tests, nail-through-the-battery tests, and incineration tests than information about discharge characteristics.

Large LiSO_2 cells with high discharge rate capability have safety devices such as high temperature fusible links, over-pressure safety vents, and time delay fuses to prevent catastrophic rupturing (battery manufacturers apparently do not like the term explosion).

The capacity of LiSO_2 cells is about 25% less than its major competitor, lithium thionyl-chloride (LiSOCl_2). LiSO_2 cells have excellent storage characteristics, and maintain a high percentage of capacity over a wide temperature range. Typical cell sizes range from 300mAh upwards to many tens of ampere hours. The open circuit voltage is about 3.0V, and the voltage during discharge is relatively flat.

Lithium thionyl-chloride (LiSOCl_2)

Presently the highest energy density system available, LiSOCl_2 is the choice over LiSO_2 in many new applications. In general, LiSOCl_2 cells have about 1/3 more capacity for a given volume or weight than do LiSO_2 cells, but energy densities vary slightly between manufacturers.

Typical cell capacities range from several hundred mAh through 20Ah, but there are cells up to 8,000 ampere hours available. See "Lithium cells suit high-energy military needs", Don Powers, EDN April 85. The open circuit voltage is 3.9V, and the discharge voltage is a constant 3.5 to 3.9V, depending on the discharge rate. High discharge rate D size cells can be operated up to 10A.

Lithium Poly-Carbonmonofluoride (LiCFn)

These are available in both coin cells and cylindrical cells up to 1.2Ah. LiCFn cells are well suited for CMOS RAM backup applications since the self discharge rate is typically only 0.5% per year of storage at room temperature. The cylindrical cells have a high pulse current capability of 1A from a 1.2Ah 2/3A cell (17mm diameter by 33.5mm high, 13.5 grams).

Secondary Batteries

The two most popular rechargeable chemistries are lead acid and nickel cadmium.

Nickel Cadmium

Nickel Cadmium, or NiCad, cells and batteries are available in sizes from about 10mAh to over 10Ah, with a wide variety of packaging styles. 10mAh to 150mAh batteries designed for memory backup are available with pins for

are really repackaged sub-C or C cells, and both have the same 1.2Ah rating as industrial grade sub-C cells. Industrial grade C cells have around 2.5Ah capacity, and D cells about 4Ah to 4.8Ah. 9V NiCad batteries come in both 6 cell and 7 cell versions, with nominal terminal voltages of 7.2V and 8.4V respectively. Since the output discharge characteristics is very flat, even a 7.2V output voltage is in most applications an adequate replacement for the 9.5 to 6V output of a 6 cell LeClanche or alkaline battery. NiCad 9V batteries, though, have only 65mAh to 100mAh capacity, much lower than the 500+mAh ratings of alkaline 9V batteries.

Sealed C and D cells are typically recharged at the 0.1C rate for 14 hours. NiCad batteries in memory backup applications are usually continuously current trickle-charged at 0.002C to 0.1C (where C is the cell's rated capacity). Standard cells are normally charged at 0.1C for 14 hours, since this allows a very simple charging circuit -- batteries can be overcharged at 0.1C for extended periods without drastic reductions in life. Special, fast rate batteries can be recharged in 20 minutes with a charge rate of 4C, but high rate chargers must have sophisticated methods of detecting end-of-charge, such as sensing the increase in temperature that occurs when full charge has been reached. Other methods of terminating fast-charge include temperature compensated voltage detection, and detection of the voltage reduction that occurs after full charge has occurred.

Cell capacity is typically reduced to 50% of its initial value after 500 to 1500 deep discharge cycles, or after 5 or more years of continuous trickle charge at 0.005C. NiCad batteries have a self-discharge rate of 0.5% per day at 23°C when near full charge, and retain 20% to 40% capacity after 5 months. At 30°C, 50% to 80% charge is retained after 30 days.

The open circuit voltage of a fully charged NiCad cell is about 1.3V, and the discharge voltage is $1.24V \pm 100mV$ for virtually the entire discharge cycle. After the cell voltage has fallen to around 1.1V, the rate a change of the cell voltage increases rapidly. Cells may be completely discharged without damage, but reverse charging at more than -200mV for extended periods will permanently damage cells. This reverse charge condition most often occurs in multi-cell batteries in which the capacity of the various cells is not well matched.

NiCad batteries come in both sealed and vented types. A sealed cell is a closed environment, and allows the escape of gas only under abnormal conditions which cause safety vents to open. The vented cell allows gases to escape from the cell during normal operation. Sealed cells are most common in the sizes from D cell and below, while vented cells are used in very large batteries in such applications as engine starting and mobile X-Ray equipment. Vented cells must be periodically inspected and the electrolyte replenished.

Lead Acid Batteries

Lead acid cells come in many forms, the most common one being the automobile battery, which is typically a vented lead-acid battery. Smaller cells, such as D and X come in fully sealed packages. Typical sealed lead-acid battery capacity is 2.5Ah (10hr rate) for D cells, and 5Ah for X cells. The open circuit voltage of a lead-acid cell can be used to estimate the charge state. For a Cyclon brand cell from Gates, the 25°C open-circuit battery voltage is about 2.18V when fully charged, declining linearly to about 1.98V when 10% of capacity is left.

The minimum voltage allowed during discharge is normally 1.6V, and lead-acid batteries should not be allowed to self-discharge below 1.8V. If allowed to self-discharge below 1.8V while in storage, the battery will take longer than normal to recharge and the next discharge cycle cannot deliver the rated capacity. Subsequent cycles, however, will result in an increase in capacity to the rated capacity. As with all batteries, the rate of self discharge is a strong function of temperature. At 5 months of storage at 20°C, the typical battery will have 60% capacity remaining. At 40°C, however, the battery would be fully discharged after 5 months.

Lead-acid batteries have extremely low internal impedance, and D cells can deliver up to 100A for short periods of time.

Since the terminal voltage of a lead-acid battery rises sharply as it nears 100% charge, the most common charge circuit is a simple constant voltage supply. A constant 2.35V charge will recharge a battery to 90% within 2 hours, and the battery can be left float charging at 2.35V indefinitely to maintain full charge. If the battery temperature will vary significantly, the float voltage should have a temperature coefficient of -2.5mV/°C/cell. Typical float life is 5 to 8 years at 25°C and 2.35V float voltage, decreasing to 2 years for 2.35V float voltage at 50°C.

For deep discharge service that need a fast cycle time, the charge voltage can be increased to 2.45V to 2.7V for even faster charging, but continuous float charging at more than 2.4V is not recommended. Typical cycle life is 2500 charges for full discharge, and over 1000 for a 25% depth-of-discharge. It is important to fully recharge lead-acid cells, with a 2.35V optimum for batteries that are cycled once per week, and 2.45V for batteries that are cycled once per day.

The cell chemistry is available in sizes from 30mm to over 100mm. LSCC cells do not require the voltage display phenomenon sometimes seen in LSCC and LSCC cells.

Lithium Polymer (Lipo) Cells
This is the most mature of the high energy density technologies. The lithium chemistry has been extensively used in military applications such as night vision devices and cameras. Early LSCC had some safety problems, but manufacturers have extensively tested their designs. Indeed, many data sheets have now mentioned about 1000 full-rate cycles, the battery life, and sometimes less than information about discharge characteristics.

Large LSCC cells with high discharge rate capability have safety devices such as high temperature fusible links, over-pressure safety vents, and fire delay fusible elements. Cathodic protection (battery manufacturers apparently do not like the term explosion).

The capacity of LSCC cells is about 20% less than in prior generations. Lithium hexafluorophosphate (LSCC) LSCC cells have excellent storage characteristics and maintain a high percentage of capacity over a wide temperature range. Typical cell sizes range from 300mAh upwards to many tens of ampere hours. The open circuit voltage is about 3.7V, and the voltage during discharge is relatively flat.

Lithium Manganese Oxide (LMO) Cells
Presently the highest energy density system available, LSCC is the choice over LSCC in many new applications. In general, LSCC cells have about 15% more capacity for a given volume or weight than do LSCC cells, but energy densities vary slightly between manufacturers.

Typical cell capacities range from 300mAh to 1000mAh through 30Ah, but there are cells up to 8000 ampere hours available. See "Lithium Cells and High-Energy Military Weapons," Don Howard, EDN April 25. The open circuit voltage is 3.7V, and the discharge voltage is a constant 3.7V, 3.6V, depending on the discharge rate. High discharge rate D size cells can be operated up to 10A.

Lithium Polyphosphate (LPP) Cells
These are available in both coin cells and cylindrical cells up to 10Ah. LPP cells are well suited for CMOS RAM backup applications since the self-discharge rate is typically only 0.5% per year at storage at room temperature. The cylindrical cells have a high current capability of 1.5Ah SCA cell (17mm diameter by 33mm high, 13.5 grams).

Secondary Batteries

The two most popular rechargeable chemistries are lead acid and nickel cadmium.

Nickel Cadmium

Nickel Cadmium or NiCad cells and batteries are available in sizes from about 10mAh to over 10Ah with a wide variety of packaging styles. 10Ah is typical for batteries designed for memory backup, and available with flat

CMOS curbs the appetite of power-hungry dc-dc converter chips

Working with CMOS rather than the standard bipolar process cuts the typical operating current of a dc-dc converter more than a hundredfold.

Designing dc-dc converters involves two basic steps: Selecting a converter control chip and adding the required external components, such as coils, resistors, and capacitors. The efficiency of the control-circuit IC determines how well the converter does its job. For a battery-powered system, high efficiency means that battery life is extended because voltage is converted to the desired value with minimum losses. In the case of ac-powered systems, efficiency translates into cooler adjacent components.

Bipolar control chips for dc-dc converters usually pull about 12 mA, with a minimum required operating voltage of 3.5 V. Quiescent current is on the order of several hundred microamperes. In contrast, the first CMOS converter control IC drastically changes such customary values, setting new standards for these devices. The MAX630's typical operating current comes in at 70 μ A, its minimum operating voltage is merely 1.8 V, and the chip's quiescent current is a miserly 0.5 μ A.

In addition, the 8-pin device needs no base current for its n-channel MOSFET output transistor, which supplies up to 300 mW when converting 5 V to 15 V. And output power is virtually unlimited when the chip is used with one external power-boosting transistor or power MOSFET.

The chip can best be described while in action, say

in a voltage-regulating loop (Fig. 1). When 5 V is first applied, current flows through inductor L and diode D, supplying the chip with 4.4 V for startup. The desired output voltage is selected by changing the value of feedback resistors R_1 and R_2 .

Comparator 1 determines whether a specific fraction of the output voltage is equal to the 1.3-V internal reference. When the converter's output voltage is too low, the comparator's output is high and the 40-kHz oscillator pulses are allowed through the NOR gate latch, turning on output MOSFET Q_1 . As long as the output voltage is less than the desired voltage, Q_1 enables the inductor to be driven from the 5-V supply with pulses at the oscillator frequency.

Delivering stored energy

Each time Q_1 is turned on, the current increases through L, storing energy. When Q_1 turns off, the polarity of the voltage reverses across the inductor (a result of $L di/dt$). The voltage at L_x then increases until D is forward-biased and current is delivered to the output.

When Q_1 is on, the current rises linearly because $\frac{di}{dt} = \frac{V}{L}$. At the end of the on-time (14 μ s for a 40 kHz,

$$55\% \text{ duty-cycle oscillator}), I = \frac{V_{T_{on}}}{L} = \frac{5 \text{ V} \times 14 \mu\text{s}}{470 \mu\text{H}} =$$

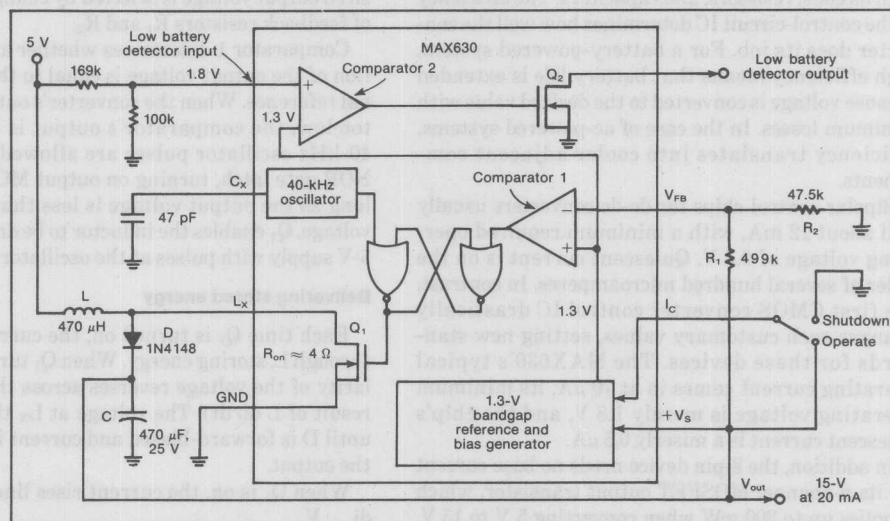
$$150 \text{ mA. The energy in the inductor is } P = \frac{1}{2} LI^2 = 5.25 \mu\text{W-s.}$$

Q_1 is turned on and off 40,000 times every second, and at maximum load the power transferred through

Charlie Allen

When the output voltage reaches the desired value, $1.31(1 + \frac{R_1}{R_2})$, the comparator's output goes low and the oscillator pulses no longer turn on Q₁. The output current is then supplied by filter capacitor C, which limits ripple to about 50 mV. As the output voltage

An n-channel MOSFET with an on-resistance of about $4\ \Omega$ and a maximum current rating of 250 mA (peak) controls the chip's output. MOSFETs have two distinct advantages over bipolar transistors. Their higher speed, which reduces switching losses and allows for smaller, lighter, and less costly magnetic components is the benefit generally mentioned with reference to high-power switchers. It must be kept in mind, though, that if a low-cost molded inductor is employed, circuit efficiency comes in at roughly 75%. An inductor with a lower series resistance, however, boosts efficiency to around 90%. In highly efficient low-power dc-dc converters, the advantage is that MOSFETs require no base current. Alternatively, their bipolar kin must use a portion of the input power for that purpose, reducing circuit efficiency. The accompanying power loss is most evi-



1. Using the MAX630 in a voltage-regulating loop delivers 15 V from a 5-V source. The divided output voltage is applied to comparator 1, where it is checked against the 1.3-V reference voltage. The comparator output enables the oscillator pulses, turning on Q₁ and allowing current to store energy in inductor L. When Q₁ is off, that energy is applied to the output.

dent in voltage-boosting systems, such as up-converters. In fact, the chip's low operating current and MOSFET output control features superior efficiency in such applications. A chip carrying a bipolar transistor, though, could use up to 10% of the total input power.

The oscillator frequency is determined by a single external component, a low-cost ceramic capacitor. A 47-pF capacitor sets the frequency to 40 kHz, a reasonable compromise between the smaller switching losses associated with lower frequencies, and the smaller inductor found at higher frequencies.

On-chip convenience

Two of the converter's features simplify power supply design—a low-battery detector and a shutdown mode. Specifically, the first compares the voltage on the Low Battery input with the internal 1.3-V reference. The detector's output is an open-drain n-channel MOSFET. The low-battery detector is also called into play in other voltage-monitoring oper-

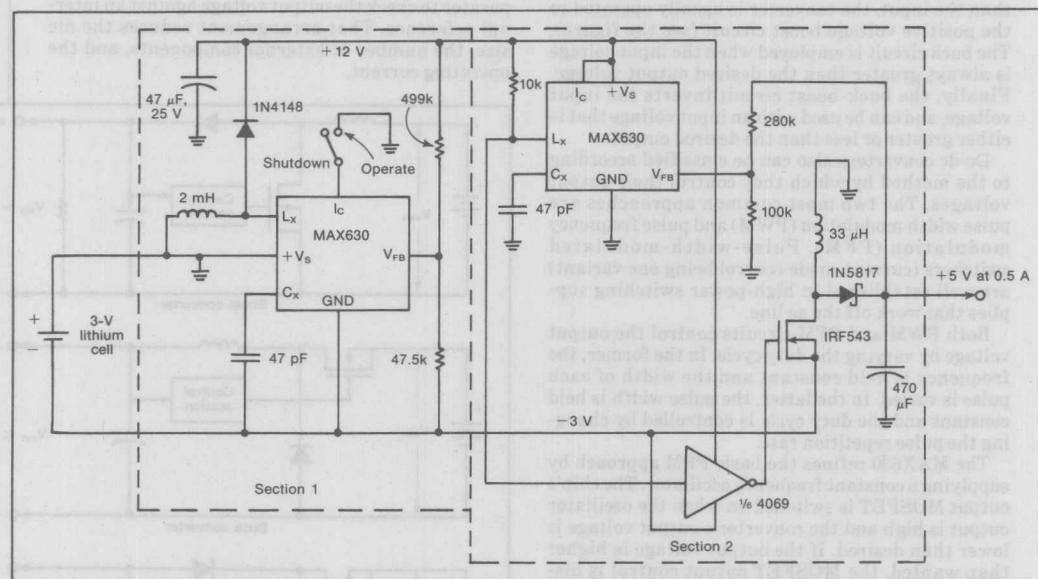
ations such as determining ac line-power failure in battery-backed systems.

The second feature employs the I_c pin to shut down the device. When in that state, the chip turns off the analog bias generator and draws less than 1 μ A of quiescent current. The shutdown condition is entered whenever the I_c pin is left floating or is driven below 1 V.

Some battery-powered systems, however, call for short bursts of high current. The extra circuitry designed to meet that need (Fig. 2) converts -3 V to $+5$ V in the buck-boost or flyback mode (see "Dc-dc Converter Configurations," p. 178).

The left half of the circuit is similar to that of the 5-to-15-V converter, and supplies 15 V for the gate drive of the external power MOSFET. This gate drive ensures that the external power MOSFET is fully turned on and presents a low resistance.

The right half of the circuit is a -3 V to $+5$ V buck-boost converter. An advantage of this circuit is that when the chip is turned off the output falls to



2. High current for short periods is obtained by adding a second section to the basic dc-dc converter. The first section furnishes a 15-V output from a -3 -V lithium cell and controls an external power MOSFET. The second is a buck-boost converter, which supplies $+5$ V from -3 V.

0 V. On the other hand, in the standard boost circuit (Fig. 1 again), the output is $V_{BATT} - 0.6$ V with the chip shut down. Also, when the buck-boost converter is shut off, it draws less than $10 \mu\text{A}$.

The inductor and output filter capacitor values have been changed to accommodate the increased power levels. At the indicated values, the circuit supplies up to 500 mA at 5 V, with an efficiency of 85%.

An alternative approach to high power conversion (-3 V to $+5$ V) uses a single chip and an inductor with two windings. One winding supplies 10 to 15 V

that drives the power MOSFET gate; the second winding delivers power for the 5-V output. Since the MOSFET gate drive is only the battery voltage minus one diode drop during startup, the MOSFET must be a low threshold device. On the other hand, the circuit that pairs up the converter chips will start and operate with power MOSFETs that have high threshold voltages.

The converter IC ensures a continuous supply of regulated $+5$ V, and automatically switches over between line power and battery backup (Fig. 3). When

Dc-dc converter configurations

Dc-dc converters come in three basic topologies: buck, boost, and buck-boost—each of which meets a particular need. When the output voltage is greater than the input, the converter is usually operated in the positive voltage boost circuit (see the figure). The buck circuit is employed when the input voltage is always greater than the desired output voltage. Finally, the buck-boost circuit inverts the input voltage, and can be used with an input voltage that is either greater or less than the desired output.

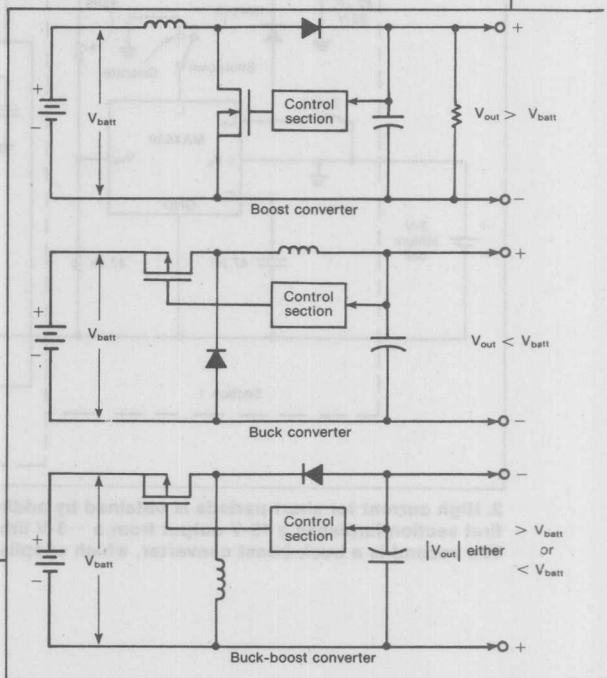
Dc-dc converters also can be classified according to the method by which they control their output voltages. The two most common approaches are pulse width modulation (PWM) and pulse frequency modulation (PFM). Pulse-width-modulated switchers (current-mode control being one variant) are well established in high-power switching supplies that work off the ac line.

Both PWM and PFM circuits control the output voltage by varying the duty cycle. In the former, the frequency is held constant and the width of each pulse is varied. In the latter, the pulse width is held constant and the duty cycle is controlled by changing the pulse repetition rate.

The MAX630 refines the basic PFM approach by supplying a constant frequency oscillator. The chip's output MOSFET is switched on when the oscillator output is high and the converter's output voltage is lower than desired. If the output voltage is higher than wanted, the MOSFET output control is disabled for that oscillator cycle. This "pulse skipping" varies the average duty cycle and thus controls the

output voltage.

Unlike the PWM ICs that use an op amp as the control element, the converter chip uses a comparator to check the output voltage against an internal reference. That arrangement reduces the die size, the number of external components, and the operating current.



the line-powered input voltage is 5 V, it furnishes 4.4 V to the chip and trickle charges the battery. The device runs continuously, boosting the 4.4 V to 5 V. When that line-powered 5-V input falls below the 3.6-V battery voltage, the battery supplies the power to the chip. The converter boosts the battery voltage to 5 V, delivering a continuous dc supply to the uninterruptible 5-V bus. Since the 5 V output is always supplied through the chip, there are no power spikes or glitches during power transfers.

Keeping an eye on the battery

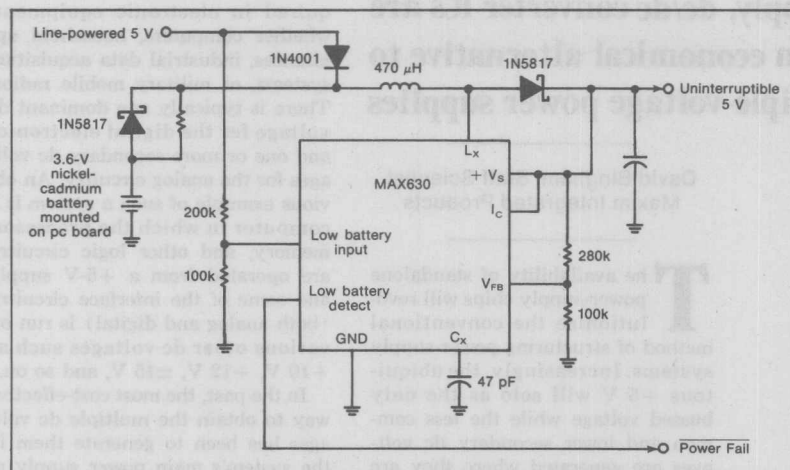
The device's low-battery detector monitors the line-powered 5-V line, and the low-battery detector output can shut down unnecessary sections of the system during power failures. Alternatively, the low-battery detector could monitor the Nicad battery voltage and warn of loss of power when the battery is nearly discharged.

Unlike battery backup systems that use 9-V batteries, this circuit does not need 12 or 15 V to recharge the battery. Therefore, it can be used to supply a 5-V

backup for modules or circuit cards on which only a 5-V supply is available.

A common problem in large electronic systems is that, although multiple power supply voltages are used, they are not always available where they are needed. Often only +5 V is distributed, but one section or printed circuit card needs both +5 V and +15 V. The ready availability of power converters enables the designer to have the needed voltage available at his fingertips. □

Charlie Allen has served as the applications engineering manager at Maxim for the past year and a half. Before that, he held the equivalent position at Intersil. He received a BSEE from Michigan State University and has published several technical articles in the past few years.



3. The MAX630 also acts as an uninterruptible 5-V power supply. It converts either the line-powered 5 V or the 3.6-V Nicad battery input to 5 V. The Power Fail output goes low when the line-powered 5-V input fails.

Chip-level converters administer local dc dosages

Whether operated from a battery or an off-line power supply, dc/dc converter ICs are an economical alternative to multiple-voltage power supplies

David Bingham, Staff Scientist
Maxim Integrated Products

The availability of standalone power-supply chips will revolutionize the conventional method of structuring power-supply systems. Increasingly, the ubiquitous +5 V will solo as the only bussed voltage while the less common and lower secondary dc voltages are generated where they are needed by dc/dc converter ICs. For the moment, these chips and their menage of external parts will remain

board-level circuitry, but the industry is gravitating toward generating the secondary voltages right on the chips that need them.

Putting an end to overkill

Almost without exception, multiple dc power-supply voltages are required in electronic equipment, whether computers, household appliances, industrial data acquisition systems, or military mobile radios. There is typically one dominant dc voltage for the digital electronics and one or more secondary dc voltages for the analog circuitry. An obvious example of such a system is a computer in which the processor, memory, and other logic circuitry are operated from a +5-V supply and some of the interface circuitry (both analog and digital) is run off various other dc voltages such as +10 V, +12 V, ± 15 V, and so on.

In the past, the most cost-effective way to obtain the multiple dc voltages has been to generate them in the system's main power supply at power levels that exceed what is actually needed for many applications. Today's more cost-effective strategy involves conscripting dc/dc converter ICs to convert the main (bussed) dc power-supply voltage into the required secondary voltage(s). Typically, the converter ICs are mounted on the same board with the circuitry that requires the non-standard power-supply voltages. It's a practical maneuver thanks to a

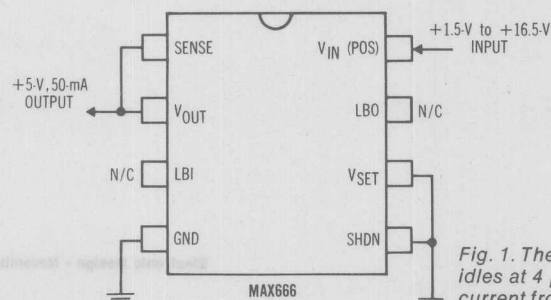


Fig. 1. The MAX666 is a CMOS linear regulator that idles at 4 μ A yet can deliver an output current from 5 μ A to 50 mA.

new series of CMOS dc/dc converter ICs that Maxim recently introduced. Intended for low- to medium-power applications, each member of this new chip battalion integrates most of the components or glue that was needed by earlier-generation converters. This results in a low component-count design, high power-conversion efficiency, simplicity of use, and low cost. Because of their high efficiencies in particular, these novel dc/dc power-supply circuits are a wise choice for battery-operated military systems—or for any other battery-operated system for that matter.

Linear, switcher, or charge pump

Maxim's family includes the three basic types of dc/dc converter circuits: the linear regulator, switcher, and charge pump. Before choosing between them, designers should be aware of the advantages and disadvantages of each, as outlined in Table 1. Because none can fulfill the needs of every application, each has

found its niche—a situation unlikely to change for some time to come.

The linear regulator in particular was the first to show up extensively in electronic equipment. It has a fine pedigree, initially being integrated onto silicon in the mid 1960s by Fairchild Semiconductor in the now famous $\mu A723$. Subsequent generations of linear regulator ICs have extended the level of available output power and, because of this higher integration, have culminated in three-terminal regulator ICs that require few, if any, external components.

More recently, CMOS technology has brought about a reduction in the quiescent (idling) current of linear regulators. For example, Maxim's MAX663 and MAX666 ICs have slashed this current to 4 μA typ so that the only real power loss occurs in output pass transistors. In addition, the MAX666 has an output current that can range from 5 μA to 50 mA, and includes alluring goodies

like shutdown, low-voltage detection, and output current limiting (see Fig. 1). A new feature, dual mode operation, proffers selection of either a fixed 5-V output or—with the addition of two external resistors—any output voltage from 2 to 15 V.

In general, linear regulator ICs are most suitable for the battery operation of equipment, such as running a 5-V system from a 9-V battery. Figure 2 shows a battery-backup power supply using a MAX666 and a 9-V transistor radio battery. Resistor R_8 senses the unregulated dc from the line supply and inhibits the output of the MAX666. A detector informs the system if the backup battery is malfunctioning. The quiescent current drawn from the battery is typically 3 to 4 μA . If a nickel cadmium stack is used, then the optional charging circuit of R_1 and diode D_2 may be added.

Linear regulators are also prudent where noise suppression is important. Other uses include the generation of say +10 V or +12 V from an existing +15-V supply at the board level rather than at the main power supply.

The two drawbacks of the linear regulator are its low power-conversion efficiency and the fact that its output voltage is always less than its input voltage. If the ratio approaches unity, then power conversion efficiencies will be proportionately high. For an efficient regulator such as the MAX663 the power conversion efficiency, assuming equal input and output currents, is:

$$\text{Efficiency} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times 100\%$$

This works out to an efficiency of approximately 50%, assuming, say, a 10-V input and a 5-V output.

Switching regulators are more efficient than linears. If a switching regulator is used to convert, say, +15 V into +5 V, then the conversion efficiency will be about 80%. The figure for a linear regulator is 33% using the formula shown $(5/15 \text{ V}) \times 100\%$. Hence, switchers are called upon extensively for high-efficiency dc/dc power conversion,

Table 1. Comparison of Dc/dc Converters

Feature	Linear regulation	Charge pump	Switcher
Output voltage regulation	Excellent	Poor	Excellent
Voltage step-up	No	Yes, but only in discrete multiples of input voltages	Yes
Voltage step-down	Yes	Yes, but only in discrete fractions of input voltage	Yes
Current step-up	No	Yes, but only in discrete fractions of input current	Yes
Power conversion efficiency	Poor	Excellent - can approach 100%	Good 80%
High power control	Yes	Not suitable	Excellent
Inductor required	No	No	Yes
Output noise	Low	Includes clock frequency plus harmonics	Includes clock frequency plus harmonics, hf hash
Minimum of external components	0	2 capacitors	1 inductor 1 capacitor

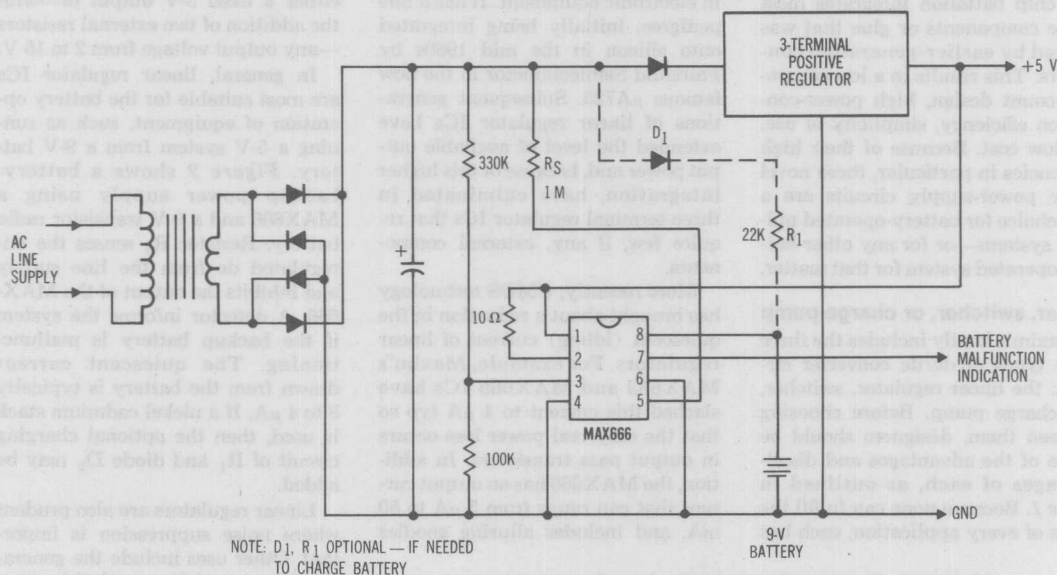


Fig. 2. This uninterruptible +5-V power supply is constructed around a MAX666 and a 9-V battery. If ac power is lost, then the MAX666 will convert the battery voltage into +5 V. The chip's low-battery detector circuitry informs the system if the backup battery is malfunctioning.

and they have the added assets of being smaller and cheaper. (Note that off-line switching power supplies are basically dc/dc converters since the ac line voltage, after being rectified and smoothed somewhat, is connected to the input of a dc/dc converter from which the desired output voltage is obtained). Also, switchers are much more versatile than both linear regulators and charge pumps and are particularly fine where stepup and voltage inversion with reasonable precision is required. (They do, however, cost more than linear regulator ICs.)

A switching power converter, unlike the linear regulator, operates in a discontinuous mode. In its simplest configuration—a two-phase mode—energy is taken from an input power source and stored in the magnetic field of an inductor in one phase. At the end of this phase a current, I , will be flowing in the inductor, L , which will have a stored energy of $\frac{1}{2} LI^2$. At the beginning of the second phase, the inductor is reconnected through a switch to the output reservoir capacitor. The current will have a value of I at the beginning of the second phase and will

either approach or decrease to zero at the end of it. Energy will thus be transferred from the magnetic field of the inductor to the reservoir capacitor. The function of this capacitor is to store the packets of energy received and produce a constant voltage during each complete period of operation. Thus the switcher requires at least two external storage elements—an inductor and a capacitor—because large amounts of energy still cannot be stored on a monolithic IC.

Although the internal operation of the switcher is discontinuous, as viewed from the output load it appears to be continuous. Furthermore, the switcher is extremely flexible in function because of the diversity of ways—called topologies—that the inductor(s) can be connected to the input supply and to the output.

Among switching regulator ICs, the MAX631 is typical of what can now be achieved using conventional CMOS (see Fig. 3). Its utility lies

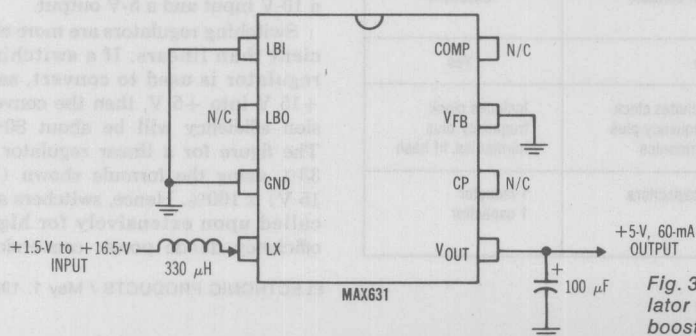


Fig. 3. The MAX631 switching regulator serves well as a voltage booster. It can supply a +5-V output voltage from an input voltage as low as +1.5 V.

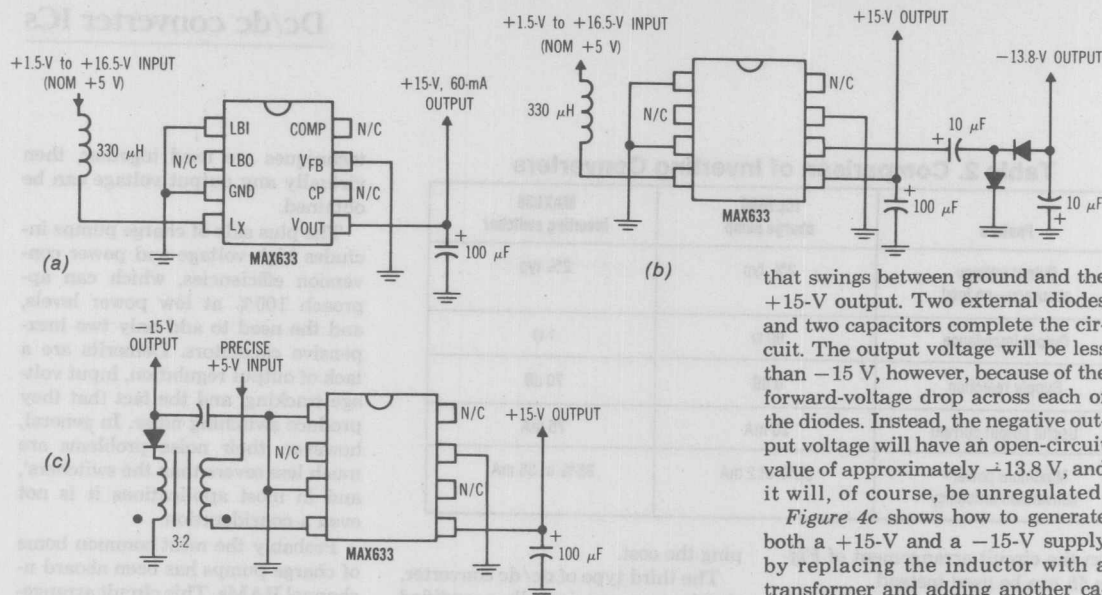


Fig. 4. Boosting a nominal input of +5V to +15 V is an easy job for the MAX633 switcher (a). If a second—but less accurate—higher voltage is needed, then the circuit shown in (b) can be used to derive both +15 and -13.8 V from a nominal +5-V input. Dual ± 15 -V supplies can be had by using a more precise +5-V input (c).

in its ability to boost a voltage as low as 1.5 V up to +5 V. All of the necessary circuit components except those storing energy (the inductor and reservoir capacitor) are contained on chip. From an applications point of view the MAX631 switcher duplicates the niceties of the MAX666 linear converter. Both have low-voltage detectors, operate with minimum quiescent currents, and feature dual mode operation.

The MAX632 and MAX633 are sister chips to the MAX631 and can be drafted to boost a 1.5-V input to +12 and +15 V, respectively. Using the circuit of Figure 4a, designers can enlist the MAX633 when a regulated +15 V is needed and a nominal

+5 V is available. The only additional components are an inductor and a capacitor. This same circuit could also operate from a two-cell battery stack to provide +5 V using the MAX631.

Generating a negative voltage

To generate a crude -15 V in addition to +15 V, the circuit of Figure 4b can be put into service. A charge pump inverts the +15-V output (which also powers the MAX633 after the circuit has started up). It consists of an on-chip power inverter

that swings between ground and the +15-V output. Two external diodes and two capacitors complete the circuit. The output voltage will be less than -15 V, however, because of the forward-voltage drop across each of the diodes. Instead, the negative output voltage will have an open-circuit value of approximately -13.8 V, and it will, of course, be unregulated.

Figure 4c shows how to generate both a +15-V and a -15-V supply by replacing the inductor with a transformer and adding another capacitor and a diode. The accuracy of the -15-V supply will not be as good as the +15-V supply but should be adequate for most applications. Note that this circuit requires a precise +5-V input since the negative output has a power-supply rejection ratio of less than unity.

Other CMOS dc/dc converters from Maxim provide stepdown and inverting outputs, together with 12- or 15-V dual-mode output voltages of either polarity. Figure 5a shows how to derive +5 V from an input voltage range of +5.5 to +16.5 V using the MAX638 stepdown or "buck" switcher. If -5 V is needed,

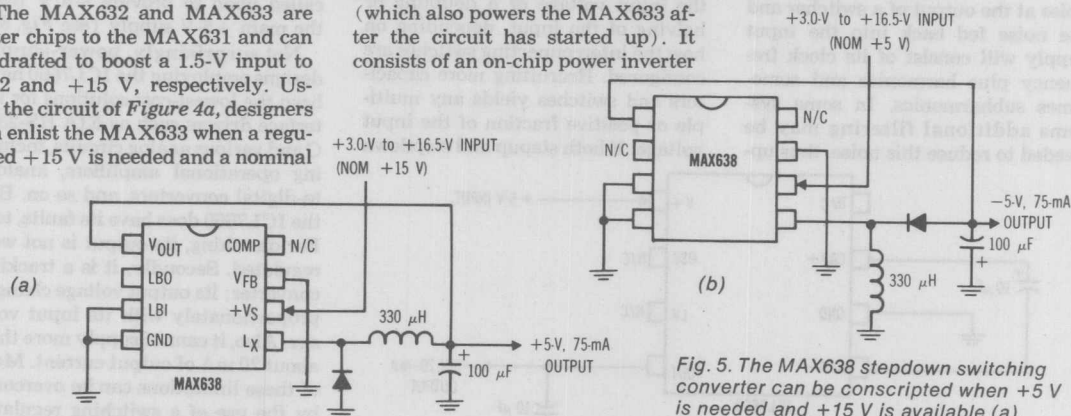


Fig. 5. The MAX638 stepdown switching converter can be conscripted when +5 V is needed and +15 V is available (a). It can also invert +5 V to -5 V (b).

Table 2. Comparison of Inverting Converters

Feature	ICL7660 charge pump	MAX638 inverting switcher
Output voltage accuracy—no load	2% typ	2% typ
Output impedance	60 Ω	1 Ω
Supply rejection	0 dB	70 dB
Useful output current	20 mA	75 mA
Maximum power—conversion efficiency	95% at 2 mA	85% at 35 mA

then the circuit arrangement of *Figure 5b* can be used instead.

One of the drawbacks of using a switcher as a low-power dc/dc converter is that an inductor is mandatory. Because inductors are the least common components in electronic equipment, designers have been reluctant to employ them. However, a wide range of inexpensive inductors from potted miniatures to small toroids are available. The potted variety resemble $\frac{1}{4}$ -W resistors and can handle milliwatts of power, while the toroids are usable at levels of several watts.

The second switcher bugbear is the fact that it produces both electrical (conducted) noise and electromagnetic (radiated) noise. The noise at the output of a switcher and the noise fed back into the input supply will consist of its clock frequency plus harmonics and sometimes subharmonics. In some systems additional filtering may be needed to reduce this noise, thus up-

ping the cost.

The third type of dc/dc converter, the charge pump, is really a modified voltage doubler—or multiplier—which has been around for 80 years. Like the switching regulator, the charge pump operates in a discontinuous mode that has two phases. In one, a flying capacitor is connected to the input supply. In the second, this capacitor is reconnected through switches to an output reservoir capacitor.

This output device serves the same function as the reservoir capacitor in the switcher—namely, to provide a continuous or dc output during both phases. The output voltage of a simple charge pump can therefore be either an inversion of the input voltage or a doubling or halving of the input, depending on how the interconnecting switches are configured. Recruiting more capacitors and switches yields any multiple or positive fraction of the input voltage. If both stepup and stepdown

techniques are used together, then virtually any output voltage can be obtained.

The plus side of charge pumps includes high voltage and power conversion efficiencies, which can approach 100% at low power levels, and the need to add only two inexpensive capacitors. Demerits are a lack of output regulation, input voltage tracking, and the fact that they produce switching noise. In general, however, their noise problems are much less severe than the switchers', and in most applications it is not even a consideration.

Probably the most common home of charge pumps has been aboard n-channel RAMs. This circuit arrangement generates on chip a voltage of -3 to -4 V from the $+5$ -V power-supply rail. The negative voltage can then back-bias the substrate, which effectively reduces junction capacitances to improve switching speeds.

Standalone converters

More recently, CMOS charge pumps have become available as standalone ICs, the trailblazer being the ICL7660. Since its introduction in the late '70s, the ICL7660 has been used by the millions for the local generation of a negative voltage from a system's main (positive) power source. It is most frequently called upon to provide -5 V from the main $+5$ -V supply (see *Fig. 6*).

Not surprisingly, power-supply designs employing the ICL7660 have been the lowest-cost solutions for interface drivers such as EIA RS-232-C and various analog circuits, including operational amplifiers, analog-to-digital converters, and so on. But the ICL7660 does have its faults, too. For one thing, its output is not well regulated. Secondly, it is a tracking converter: its output voltage changes proportionately with its input voltage. Also, it cannot supply more than about 20 mA of output current. Most of these limitations can be overcome by the use of a switching regulator such as the MAX638. *Table 2* compares the features of the MAX638 with those of the ICL7660.

New CMOS charge-pump ICs have been slow in arriving because

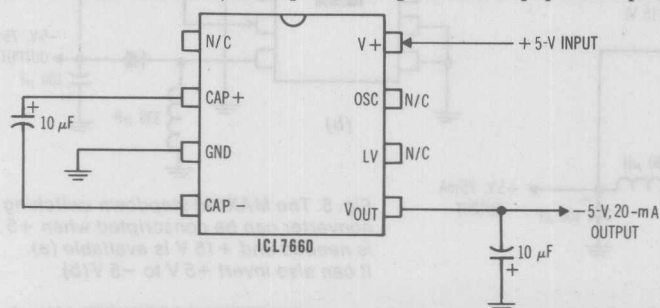


Fig. 6. The ICL7660 charge-pump converter, together with two external capacitors, can be employed to derive -5 V from a $+5$ -V supply. However, it is a tracking converter and has an output that is poorly regulated.

Dc/dc converter ICs

of their susceptibility to latchup—a nuisance that occurs in a CMOS circuit when its inputs or outputs are forward biased, tripping the device into a high-conductance state similar to a conducting SCR. This condition can only be remedied by removing the input power supply—not a very practical solution. But latch-up mechanisms are now much better understood by IC makers, who can take steps to guard against it. New charge-pump ICs such as the MAX680 tap both positive and inverting pumps to supply ± 10 V from a +5-V input. Looking ahead, the improved CMOS charge-pump circuitry will have a dramatic effect in another arena, as well.

Included on chip

Certain standard IC functions require an unusual—but not necessarily highly accurate—dc power, supply voltage(s). Take, for example, RS-232-C line drivers whose outputs must drive a load to approximately ± 10 V. These voltages are not critical but must be within a range of ± 5 to ± 15 V. Increasingly, where the market for such an IC is sufficiently large and the economics amenable, chip makers are going to include a dc/dc power converter right on the same chip. Charge pumps are a practical choice for such converters owing to their high power-conversion efficiency, low power levels, and low cost.

The MAX232 pioneers a new series of ICs that include their own power supplies. The chip's two RS-232-C transceivers have been integrated along with a double charge pump to enable operation from a single +5-V supply. Four external capacitors—two for each charge pump—must be connected to the MAX232.

But external capacitors are not needed by the MAX233, which is a hybrid packed into a 20-pin DIP along with a modified MAX232 that uses a high on-chip chopper frequency plus a proprietary lead frame. □

DC/DC converters adapt to the needs of low-power circuits

High cost, quiescent current, and circuit complexity have often restricted switching power supplies to high-power applications, for which the switchers' high efficiency, wide input range, and reduced size and weight offset their drawbacks. Now, however, you can employ switchers in low- and medium-power applications as well.

Len Sherman, Maxim Integrated Products

Designers of dc/dc-conversion products are now addressing the special requirements of low- and medium-power applications. As a result, you can apply switching techniques' advantages in battery-powered portable equipment, telemetry devices, and consumer products.

A key requirement for designers of battery-powered products is that they minimize the number of cells used in the product. Substituting, for example, two large cells for a stack of six or seven smaller ones yields not only reductions in size and weight but also increased reliability and energy density. An efficient, low-power step-up voltage converter used in conjunction with a few high-capacity, low-voltage cells makes such a trade feasible, especially in an application where a stack of expensive rechargeable batteries would be the alternative.

The circuits shown in Figs 1 through 7 are all

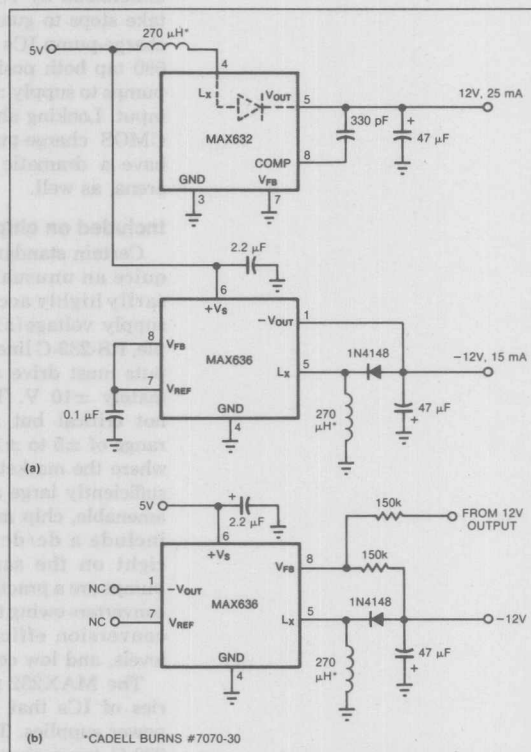


Fig 1—You can tailor this $\pm 12V$ supply to provide either independently regulated outputs (a) or a tracking negative output (b). The inductors don't exact too great a size penalty: Each measures only 0.6 in. long by 0.26 in. in diameter.

The flyback configuration keeps circuitry compact, and it adapts not only to voltage boosting but to buck and buck/boost configurations as well.

flyback-type switching dc/dc converters (the same type that generates 10- to 20-kV supplies for television, video display terminals, and oscilloscopes) that operate at 50 kHz (see box, "Flyback converters' internal operation"). The flyback configuration keeps the circuitry compact, and its versatility allows it to accomplish more than simple voltage boosting.

Derive $\pm 12V$ from digital system's supply

Often, a digital system powered by a 5V supply includes a few analog functions that require $\pm 12V$. The circuit shown in Fig 1 uses two dedicated 8-pin converters—the MAX632 and MAX636—to derive 25 mA at 12V and 15 mA at $-12V$ from a 5V logic supply. You can configure the circuit for independently regulated outputs (Fig 1a) or for tracking regulation (b).

The positive converter's efficiency is 85%; the inverter's is 75%. You can improve these efficiency figures slightly by using Schottky diodes rather than the MAX632's internal diode and the 1N4148 signal diode connected to pin 5 of the MAX636. If you opt to use a Schottky diode with the MAX632, connect it in parallel with the chip's internal diode (that is, between pins 4 and 5).

With several popular types of high-current rectifier diodes, such as ones in the 1N4000 Series, efficiency

and overall performance are poor for high-frequency (greater than 10 kHz) dc/dc conversion. Many of these diodes were designed to pass high current only at 120 Hz; therefore, they waste energy at 50-kHz operating frequencies. In addition, these slow rectifiers might also allow the inductor's discharge voltage to reach excessive levels before the rectifier turns on and directs current to the load.

Small-signal diodes, such as the 1N4148, are fast enough and work well in applications that require less than 50 mA. High-speed rectifiers, such as the 1N4935, are suitable in applications that require as much as 1A. Schottky diodes provide the best performance with respect to speed and forward voltage drop, and they can significantly improve efficiency in low-voltage, high-current applications. However, you'll have to decide on the basis of your individual application whether their higher cost and relatively low reverse breakdown voltage eliminate the Schottky diodes from consideration.

External MOSFET increases power

If your application requires higher power than Fig 1's circuit provides (if, for instance, you need the power for a data-acquisition board or a high-level industrial controller), then you can modify the circuit by adding an

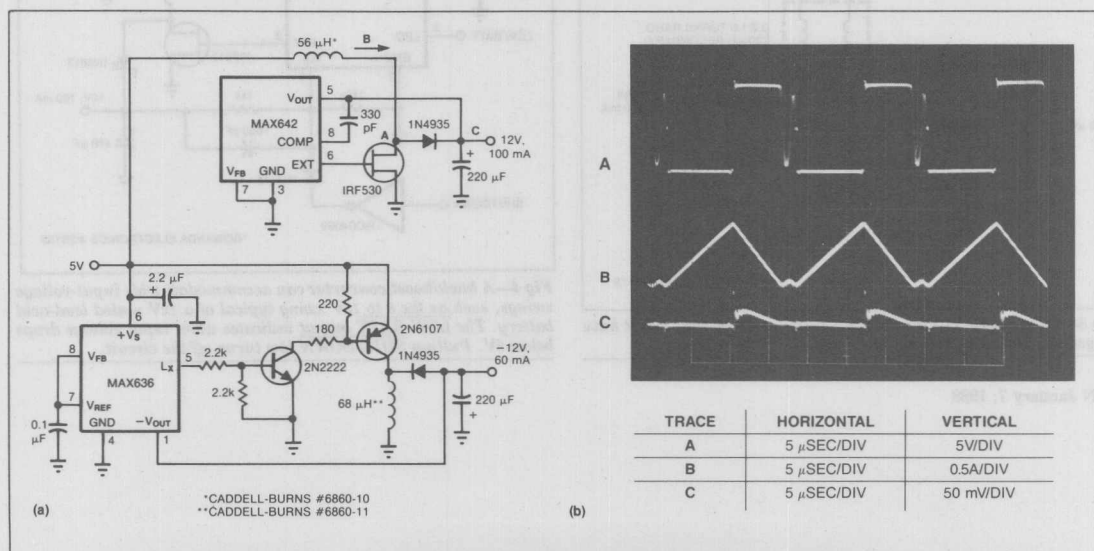


Fig 2—With the addition of a few external components (a), the circuit of Fig 1 can supply currents of 100 mA at 12V and 60 mA at $-12V$. Traces A, B, and C (b) represent the switch voltage, inductor current, and output ripple for the 12V supply.

external power MOSFET, as shown in Fig 2a, and obtain 100 mA at 12V and 60 mA at -12V. The power MOSFET drops the 12V converter's efficiency to 80%, but driving the power MOSFET doesn't require any additional parts.

The scope photo (Fig 2b) shows some of the key waveforms in the step-up circuit. Trace A is the voltage waveform at the drain of the IRF530 MOSFET (under full load), trace B is the inductor current, and trace C is the ripple voltage at the 12V output. The ringing found on trace A near the end of each discharge cycle is normal and is due to the inductor's interaction with stray capacitance when the inductor current decays to nearly zero. As you can see from trace C, this ringing has no effect on the output waveform.

Compensate for IR drops

Not only might you need to derive $\pm 12\text{V}$ from a 5V supply, you might also need to derive a regulated 5V level from a nominal 5V supply that suffers from an unacceptable voltage drop because of IR effects in long power-distribution cables. You can efficiently boost the voltage back to a regulated 5V by using the circuit shown in Fig 3.

That circuit operates at input voltages as low as 4.5V. The transformer's 3.2:1 turns ratio allows the circuit to supply more than the MAX631's usual output current without requiring external power transistors. This circuit provides as much as 150 mA of output current at 5V. You can wind the transformer on a 14 $\times$ 8-mm pot core, or you can obtain the transformer by ordering the standard part number listed in the schematic.

When the MAX631's L_X switch turns off at each half

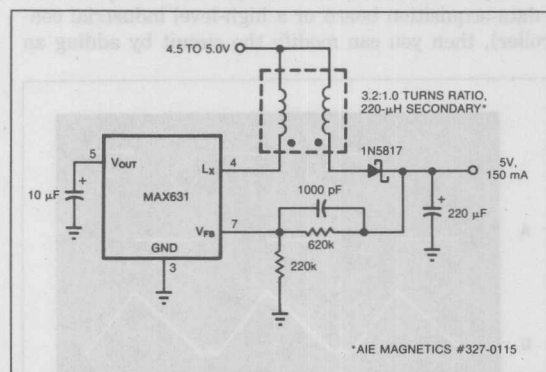


Fig 3—This simple circuit boosts a supply voltage that might have sagged substantially because of IR drops in long cables.

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cycle of its 50-kHz clock, the reflected voltage in the transformer's primary generates a 9V supply voltage for the MAX631 at the V_{OUT} pin. Operating the MAX631 at 9V rather than at the 4.5V provided at the input increases the gate-source voltage of the internal MOSFET, consequently reducing the MOSFET's on-resistance. This circuit requires the external feedback resistors at V_{FB} because, unlike the previous circuits, this circuit doesn't allow you to use V_{OUT} as the feedback input for the regulator.

Derive 12V from 8 to 15V input

The simple boost converters of the previous examples are inadequate for some battery-powered applications. For example, the unregulated output of a 12V sealed lead-acid battery varies from worst-case peaks of 15V down to as little as 8V when it is deeply discharged. Therefore, you can't derive a regulated 12V output from a 12V lead-acid battery by using a simple boost converter, such as one of those illustrated in Figs 1 and 2, because a boost converter can't accept an input voltage that is greater than its output voltage. Conversely, a buck converter can't accept an input voltage that's less than its output; therefore, a simple buck converter won't work either. A buck/boost converter, as the name implies, is a combination of buck and boost circuitry that successfully addresses the challenge of

Text continued on pg 150

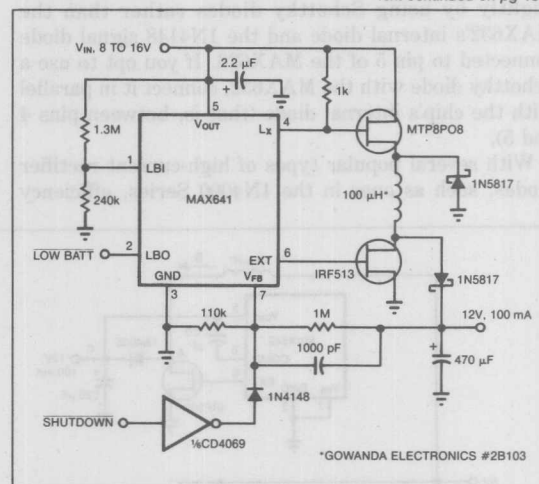


Fig 4—A buck/boost converter can accommodate wide input-voltage swings, such as the 8 to 15V swing typical of a 12V sealed lead-acid battery. The LOW BATT output indicates when input voltage drops below 8V. Pulling SHUTDOWN low turns off the circuit.

Flyback converters' internal operation

In a flyback converter, voltage applied to an inductor or transformer primary via a switch causes inductor current to rise for a fixed period of time. When the voltage is switched off, the magnetic field stored in the transformer collapses, causing the secondary to supply current to the load. With the MAX640 and MAX630 Series devices, this switching occurs at 50 kHz. You can use these devices to step up the voltage, step it down, or invert it just by changing the configuration of the switch (transistor), coil, and steering diode.

Fig A illustrates the MAX641's internal operation. When the output voltage drops below the preset (or externally set) value, the error comparator switches high and connects the internal oscillator to the L_X and EXT outputs. EXT is typically connected to the gate of an external n-channel power MOSFET (although the external MOSFET isn't necessary for most of the low-power circuits discussed in

the accompanying article). When EXT is activated, the MOSFET turns on and off at the oscillator frequency.

When EXT is high, the MOSFET switches on, and the inductor current increases linearly, storing energy in the coil. When EXT switches the MOSFET off, the coil's magnetic field collapses, and the voltage across the inductor changes polarity. The voltage at the catch diode's anode then rises until the diode is forward-biased, delivering power to the output. As the output voltage reaches the desired level, the error comparator inhibits EXT until the load discharges the output capacitor to a point at which the error comparator connects the oscillator to the L_X , and EXT generates output once again.

The MAX641 doesn't have a V_{IN} pin. Input power to start the dc/dc converter is supplied via the external inductor (and external diode, if used), to the V_{OUT} pin. If you use an external catch

diode, connect its cathode to V_{OUT} . Once the converter is started, it's powered from its own output voltage. This bootstrap design ensures that the external MOSFET has the maximum gate drive and, consequently, the minimum R_{ON} .

One external component that you must select is the inductor. Although the inductance of many types of coils, such as RF chokes and air-core inductors, frequently falls in the appropriate range for dc/dc converters (50 to 500 μ H), these inductors typically saturate at only a few milliamps and therefore are not a good choice for your dc/dc-converter design.

A saturated inductor ceases to behave as an inductor. It can no longer store energy in its magnetic field, so the mechanism that normally limits the inductor current no longer operates; all that limits the current is the series resistance. This resistance is quite low; consequently, the current can rise to an excessive, and possibly destructive, level.

The scope photo in Fig B shows the switch voltage (trace A) and inductor-current waveforms (trace B) for an inductor that's well on its way to saturation. Compare these waveforms with the normal performance illustrated in Fig 2b on pg 146. The A and B waveforms in both photos are of the same A and B nodes of the 12V boost circuit in Fig 2a. Fig B reflects the effects of using an inductor with an inadequate current rating in Fig 2a's circuit.

When you look at Fig B, you'll see that, in the middle of the

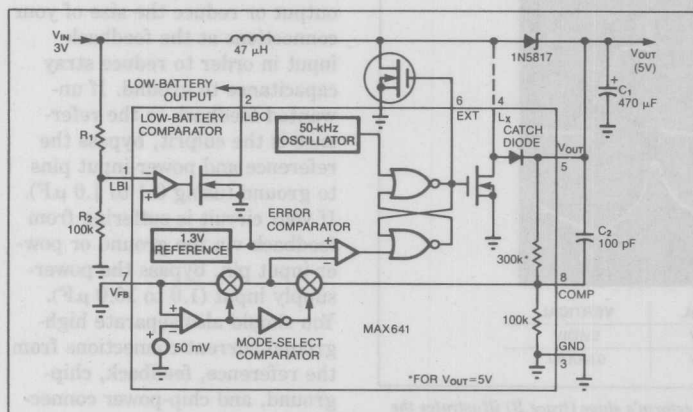


Fig A—This block diagram illustrates the MAX641's operation. For many low-power applications, the external MOSFET and Schottky diode are unnecessary.

level, the current waveform's slope increases markedly, indicating the onset of saturation. At this point, the effective inductance of the coil decreases because the current through the inductor has risen to the saturation level. The rising edge of the switch-voltage waveform is much slower in Fig B than in Fig 2b because the inadequately rated inductor takes several microseconds to come out of saturation.

An inductor doesn't saturate as long as its operating current is less than its rated maximum current. At first glance, it would seem easy enough to specify the maximum current rating for your inductor, but what you have to watch out for in your dc/dc designs is that the peak inductor current is often four to six times the converter's average current output. In the case of flyback converters, this peak current flows not just under peak load conditions, but each

on. For this reason, you must give careful consideration to the current rating of your converter circuit's inductor.

Besides the care required in the selection of inductors, another often-overlooked area of concern in dc/dc-converter design is that encompassed by grounding, shielding, and bypassing. The quality of ground connections is key to the performance of dc/dc converters. Because the peak current in an inductor or switch (transistor) can reach several amps, you must provide these points with very-low-impedance paths to the supply common. For example, in the inverting circuit of Fig 2a, the coil current typically exceeds 1A. For best results, use separate paths to ground for the high-current paths so that they are separated from the chip's power and feedback connections. If you don't have the option of separate traces, then use as heavy a sin-

carry the high current back to the supply.

Loop instabilities, caused by interactive ground connections or stray capacitive pickup, can also severely limit the performance of an otherwise sound dc/dc-converter design. Some of the symptoms of these problems are high ripple voltages at the output, efficiency that's lower than expected, and "motorboating," or low-frequency oscillation.

Motorboating occurs when the control loop of the dc/dc converter produces pulses in periodic clusters of 10 to 20 pulses rather than at more or less random intervals. Motorboating can be caused by one or more of the following phenomena: stray pickup at the feedback node, unwanted feedback to the reference, and feedback via the ground or power-input pin.

If the cause is stray pickup at the feedback node, add a lead compensation capacitor (100 to 1000 pF) from the feedback terminal or COMP pin to the circuit output or reduce the size of your connections at the feedback input in order to reduce stray capacitance to ground. If unwanted feedback to the reference is the culprit, bypass the reference and power-input pins to ground (using 0.1 to 1.0 μ F). If your circuit is suffering from feedback via the ground or power-input pin, bypass the power-supply input (1.0 to 10.0 μ F). You should also separate high-ground-current connections from the reference, feedback, chip-ground, and chip-power connections.

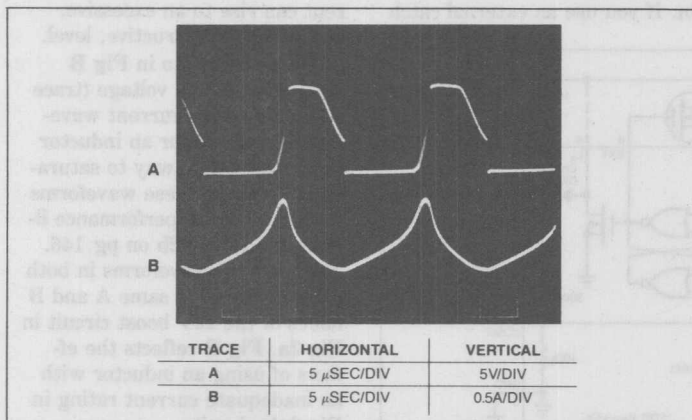


Fig B—The marked increase in the current waveform's slope (trace B) illustrates the onset of saturation for an inductor with an inadequate current rating. Trace A represents switch voltage.

You must sometimes develop 5V from a nominal 5V input that has sagged because of IR drops in long power-distribution lines.

the wide input-voltage swing associated with the sealed lead-acid battery.

The circuit of Fig 4 is a buck/boost converter that provides 100 mA at 12V and accepts 8 to 16V inputs. Both ends of the circuit's inductor are switched by separate power MOSFETs, which the MAX641 drives directly via its L_X and EXT outputs. These outputs operate out of phase, so the p- and n-channel FETs turn on at the same time. When both the n- and p-channel FETs turn off, the two Schottky diodes steer the coil's discharge current to the 12V output. A slight drawback of this circuit is that the converter's efficiency is less than that of a pure buck or boost converter, because the two MOSFETs and two diodes increase losses in the charge and discharge current paths. Nevertheless, the circuit still delivers 100 mA at a respectable 70% efficiency figure.

An additional benefit of this type of circuit is that you can control its operation with a TTL-level signal. Overriding the V_{FB} input with a high-level TTL signal (such as the diode-coupled inverter output in Fig 4) fools the MAX641's internal feedback circuitry into thinking that the output is too high, so the chip turns off both MOSFETs. The circuit's idle current is around 400 μ A.

Obtain 50V from a 12V supply

If you need to generate voltages higher than the 5 and 12V levels of the circuits shown in Figs 1 through 4, consider a configuration such as the one shown in Fig 5. It provides a 50V output from a 12V input and is simpler than Fig 4's circuit: Because the output is higher than the input, a simple boost configuration suffices.

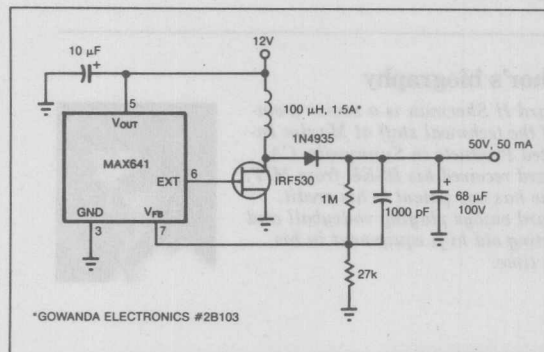


Fig 5—Only the power MOSFET, catch diode, and output-filter capacitor need to withstand high voltages in this 50V supply circuit.

The circuit uses an IRF530 n-channel MOSFET in conjunction with a MAX641 dc/dc controller. In this circuit, the 50V output is not connected directly back to the V_{OUT} pin because that pin has a maximum voltage rating of 18V. The circuit uses an external resistive divider network to provide feedback to the V_{FB} input. The V_{OUT} pin obtains power for the MAX641 directly from the 12V supply. The only components that must withstand high voltages are the MOSFET, the steering diode, and the output filter capacitor: They're rated at 100V, 200V, and 100V, respectively.

A different twist to high-voltage dc/dc conversion is the requirement to power low-voltage logic circuitry from a high-voltage source—for instance, the telephone system's -48V battery voltage. The circuit of Fig 6 uses a basic boost configuration to convert -48V to 5V. A small-signal, high-voltage pnp transistor shifts the feedback signal from the 5V output to the MAX641, whose ground terminal (pin 3) is tied to the -48V input. The output, at 5V with respect to ground, forces about 43 μ A through the 100-k Ω sense resistor and the emitter of the 2N5401. This current is sent through the 30-k Ω input resistor at V_{FB} , placing this pin 1.3V above the ground pin (or at -46.7V). Because the internal reference of the MAX641 is a 1.3V bandgap reference, the 1.3V bias level at the feedback input closes the feedback loop.

This biasing scheme allows the EXT output to directly drive the n-channel MOSFET, switching the inductor to the -48V input without level shifting of the MOSFET's drive signal. The 330-pF capacitor provides feedforward compensation, which stabilizes the regula-

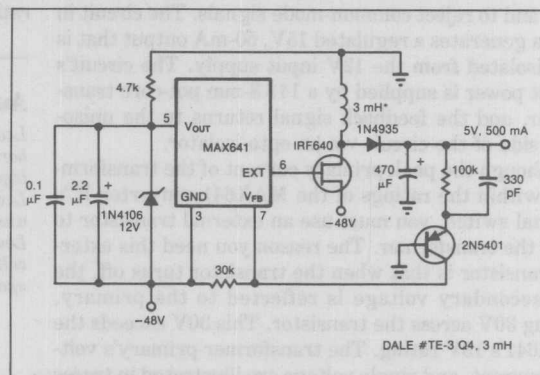


Fig 6—Telecomm applications often require you to develop your logic-level supply from -48V. Suitable for such applications, this circuit delivers 5V at 500 mA.

A buck/boost converter can deal with the wide input-voltage swings associated with sealed lead-acid batteries.

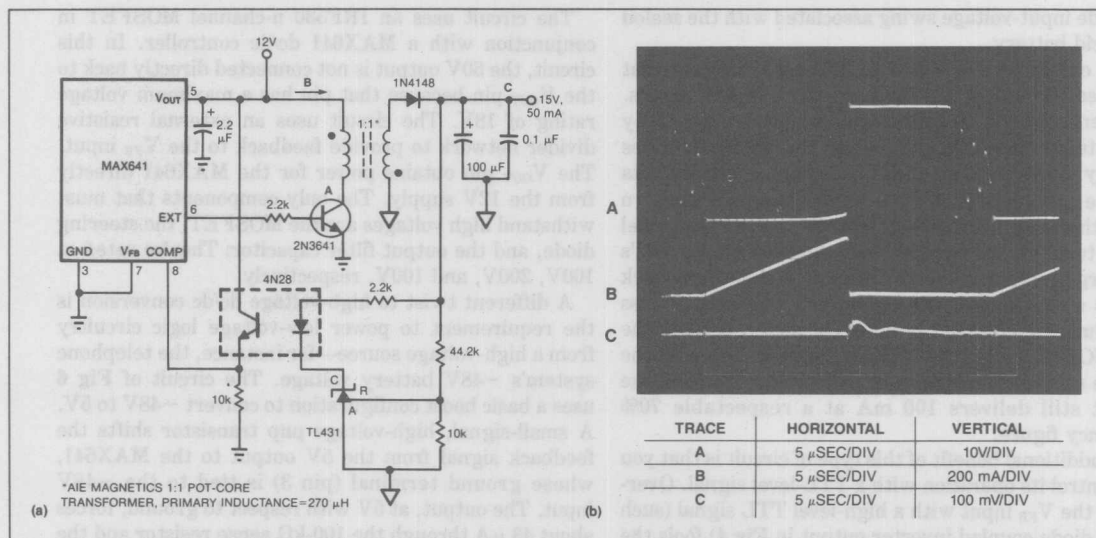


Fig 7—This circuit (a) provides 50 mA at 15V with an isolation rating of 500V—a function of the transformer and opto-isolator. In the scope photo (b), traces A, B, and C represent the switch voltage, primary current, and output-voltage ripple.

tor's control loop and improves the regulator's transient-load response.

Generating an isolated supply

In large analog systems and in industrial-control systems, you must often provide power that is electrically isolated from the main system's power source. This isolation is necessary to prevent ground loops, to protect measurement hardware from dangerous voltages, and to reject common-mode signals. The circuit in Fig 7a generates a regulated 15V, 50-mA output that is fully isolated from the 12V input supply. The circuit's output power is supplied by a 14×8-mm pot-core transformer, and the feedback signal returns to the unisolated side of the circuit via an opto-isolator.

Although the peak primary current of the transformer is within the ratings of the MAX641 converter IC's internal switch, you must use an external transistor to drive the transformer. The reason you need this external transistor is that when the transistor turns off, the 15V secondary voltage is reflected to the primary, placing 30V across the transistor. This 30V exceeds the MAX641's 18V rating. The transformer primary's voltage, current, and ripple voltage are illustrated in traces A, B, and C, respectively, of the Fig 7b scope photo.

To transmit the feedback signal across the isolation barrier, the 15V output is divided and compared with

the 2.75V reference of a TL431 shunt regulator. When the voltage at the TL431's reference input exceeds 2.75V, the TL431 draws current through the opto-isolator's photodiode. The opto-isolator's transistor then pulls the COMP input of the MAX641 high, turning off the EXT output. The COMP input connects to the MAX641's internal voltage divider, and thus the opto-isolator's transistor can control the MAX641. The components specified in Fig 7a provide an isolation rating of 500V.

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Author's biography

Leonard H Sherman is a senior member of the technical staff at Maxim Integrated Products in Sunnyvale, CA. Leonard received his BSEE from MIT, and he has one patent to his credit. Leonard enjoys playing volleyball and collecting old hi-fi equipment in his spare time.



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2-3	Extending The Voltage Rating Of The MAX850

You can extend the voltage output of the MAX680 by almost 100% and not exceed electrical limits. Figure 2-1 and 2-2 show how 5V can be turned into ± 14.5 or ± 19.5 V respectively all without the use of inductors.

In conventional applications, the MAX680 converts to ± 10 V by first doubling +5V to +10V and then inverting +10V to -10V. In this application the normal switched cap charge pump operation is followed by a doubler section for ± 19.5 V or 1/2 doubler section for ± 14.5 V outputs. The diodes must be able to switch in the range of 25ns.

The graph shows the output voltage vs. output current for both ± 19 V and ± 15 V with silicon or schottky diodes. Voltage conversion efficiency is better than 95% with no load.

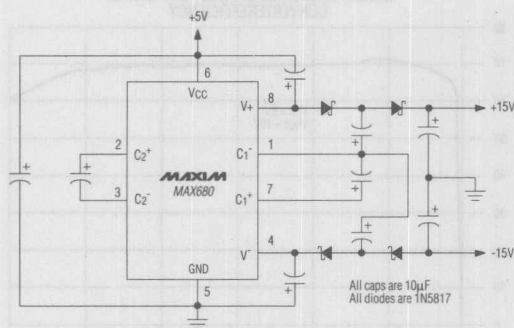


Figure 2-1.

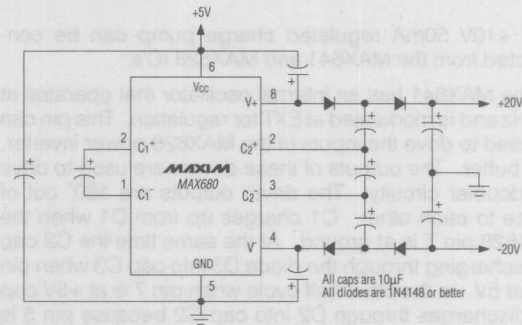


Figure 2-2.

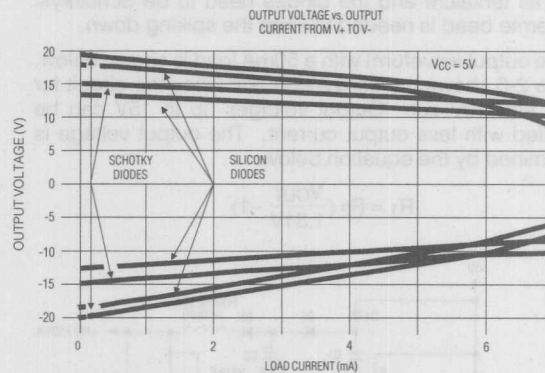


Figure 2-3.

A +10V 50mA regulated charge pump can be constructed from the MAX641 and MAX628 IC's.

The MAX641 has an internal oscillator that operates at 50kHz and is modulated at EXT for regulation. This pin can be used to drive the inputs of the MAX628 power inverter, and buffer. The outputs of these drivers are used to drive the doubler circuitry. The driver outputs are 180° out of phase to each other. C1 charges up from D1 when the MAX628 pin 7 is at ground. At the same time the C2 cap is discharging through the diode D3 into cap C3 when pin 5 is at 5V. In the other half cycle when pin 7 is at +5V cap C1 discharges through D2 into cap C2 because pin 5 is now at Ground. With this alternating action the cap C3 is recharged every 20µs.

For a 50mA output the caps need to have a low ESR such as tantalum and the diodes need to be Schottkys. The ferrite bead is needed to keep the spiking down.

The output waveform with a 50mA load is shown below. Figure 2-6 shows the conversion efficiency the circuit for 5V in and 10V out. Output voltages up to 15V can be supplied with less output current. The output voltage is determined by the equation below.

$$R_1 = R_2 \left(\frac{V_{OUT}}{1.31V} - 1 \right)$$

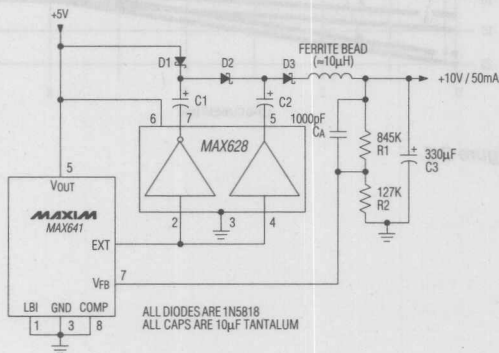


Figure 2-4.

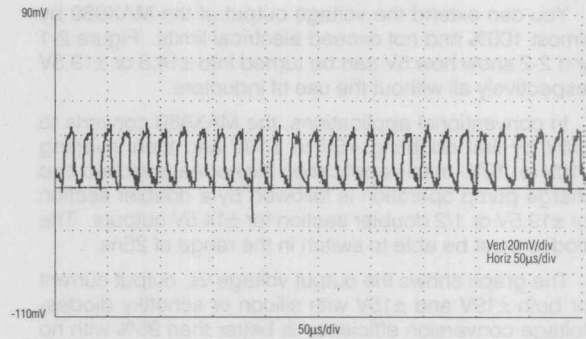


Figure 2-5. Output Noise with 50 mA Load

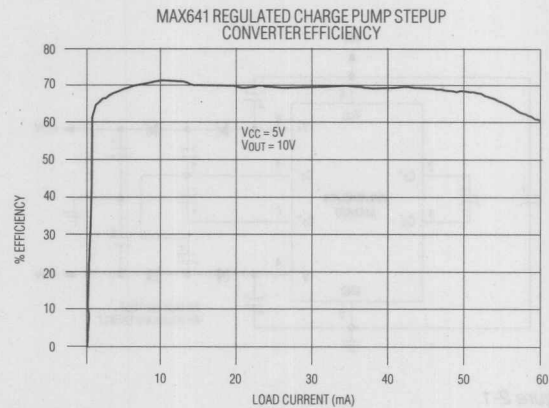


Figure 2-6.

Paralleling MAX680 Charge Pumps

Paralleling multiple MAX680s reduces the output resistance of both the positive and negative converters. The effective output resistance is the output resistance of a single device divided by the number of devices. As illustrated, each MAX680 requires separate pump capacitors C1 and C2, but all can share a single set of reservoir capacitors at V+ and V-.

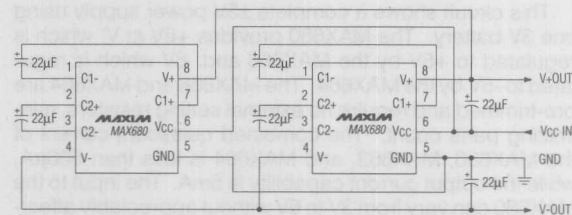


Figure 2-7.

Paralleling ICL7660s

Paralleling multiple ICL7660's reduces the output resistance. Each device requires its own pump capacitor C1, however the reservoir capacitor, C2, serves all devices. The equation for calculating output resistance is shown.

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660)}}{n \text{ (number of devices)}}$$

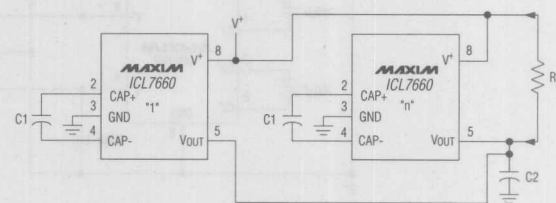


Figure 2-8.

Combined Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 2-9. In this circuit, capacitors C1 and C3 perform the pump and reservoir functions respectively to generate a negative voltage. Capacitors C2 and C4 are pump and reservoir capacitors for the multiplied positive voltage. This configuration, however, does lead to higher source impedances of the generated supplies. Due to the finite impedance of the common charge pump driver.

The output voltages are:

$$+OUT = 2V_{IN} - 2V_{FD}$$

$$-OUT = -V_{IN}$$

where V_{FD} is the forward voltage of diode D1 and D2.

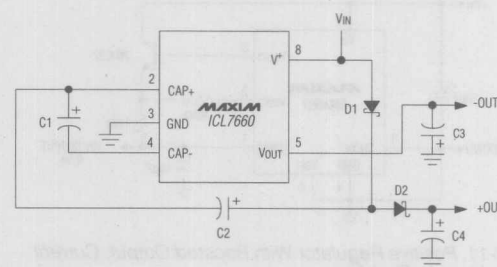


Figure 2-9.

This circuit shows a complete $\pm 5\text{V}$ power supply using one 3V battery. The MAX680 provides $+6\text{V}$ at V^+ which is regulated to $+5\text{V}$ by the MAX666 and -6V which is regulated to -5V by the MAX664. The MAX666 and MAX664 are pre-trimmed and require no external setting resistors, minimizing parts count. The combined quiescent current of the MAX680, MAX663, and MAX664 is less than $500\mu\text{A}$, while the output current capability is 5mA . The input to the MAX680 can vary from 3V to 6V without appreciably affect-

ing regulation. With higher input voltage, more current can be drawn from the outputs of the MAX680. With 5V at VCC, 10mA can be drawn from both regulated outputs simultaneously. Assuming 150Ω source resistance for both converters, with $(I_L^+ + I_L^-) = 20\text{mA}$, the positive charge pump will droop 3V, providing +7V for the negative charge pump. The negative charge pump will droop another 1.5V due to its 10mA load, leaving -5.5V at V-, sufficient to maintain regulation for the MAX664 at this current.

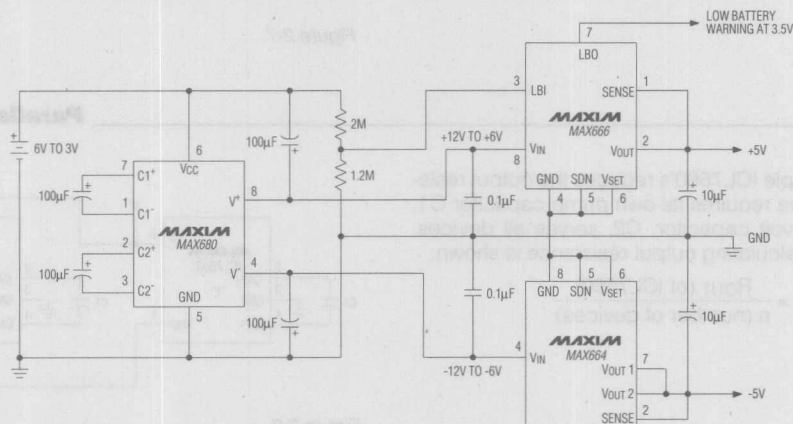


Figure 2-10.

Positive and Negative 0.5A Boosted Regulators

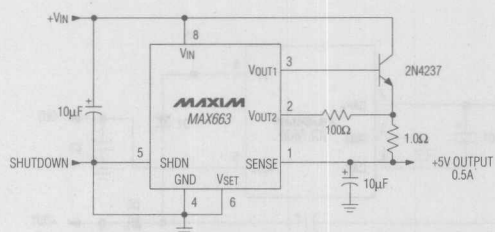


Figure 2-11. Positive Regulator With Boosted Output, Current Limit, and Low I_Q Shutdown

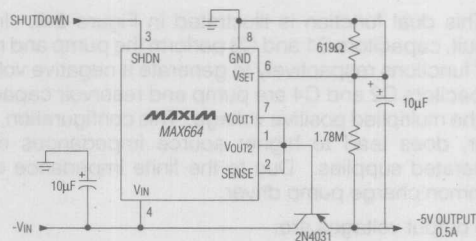


Figure 2-12. Negative Regulator With Boosted Output and Low I_Q Shutdown

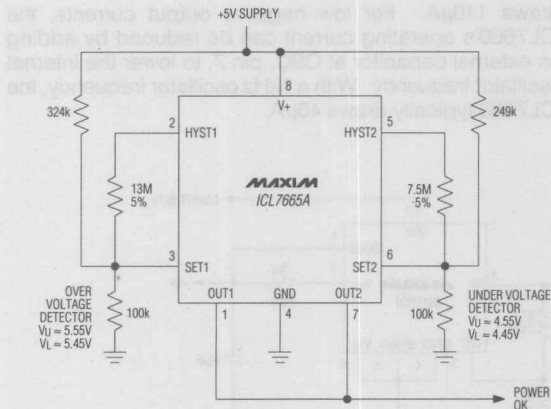


Figure 2-15. Fault Monitor for a Single Supply

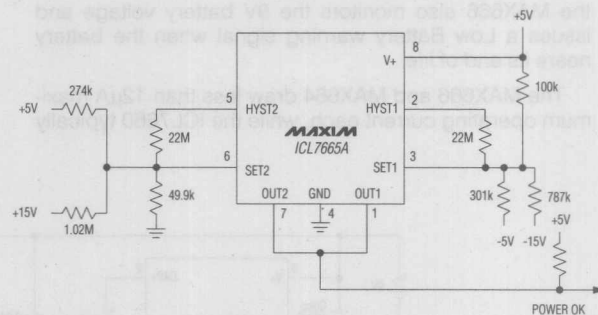


Figure 2-16. Multiple Supply Fault Monitor for ±5V and ±15V

Combination Low Battery Warning and Low Battery Disconnect

Nickel Cadmium (NiCad) batteries are excellent rechargeable power sources for portable equipment, but care must be taken to ensure that NiCad batteries are not damaged by overcharge. Specifically, a NiCad battery should not be discharged to the point where the polarity of lowest capacity cell is reversed and that cell is reverse charged by the higher capacity cells. This reverse charging dramatically reduces the life of a NiCad battery. This circuit both prevents reverse charging and also gives a low battery warning. The typical low battery warning

voltage is 1V per cell. Since a NiCad "9V" battery is ordinarily made up of 6 cells with a nominal voltage of 7.2V, a low battery warning of 6V, with a small hysteresis of 100mV, is appropriate. To prevent over discharge of the battery, the load should be disconnected when the battery voltage falls to $1V \times (n-1)$, where $N = \text{number of cells}$. In this case, low battery load disconnect occurs at 5V. Since the battery voltage rises when the load is disconnected, 800mV of hysteresis is used to prevent repeated on-off cycling.

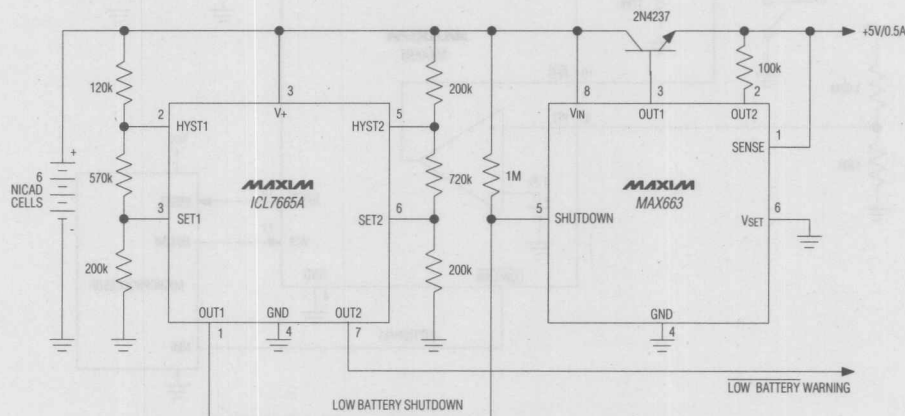


Figure 2-17.

All commercially available low drop-out positive voltage regulators use PNP bipolar transistors as pass transistors because they are easy to drive. The voltage on the base is lower than the output voltage so one can completely saturate the pass transistor (less than 0.4V drop). On the other hand the drop through the pass element of an NPN output stage will always be higher than the $V_{BE(sat)}$ drop (1.2V min), as there is generally no higher voltage available than the input voltage.

The best pass transistor (i.e. with the lowest ON resistance) would be an N channel MOSFET ($V_{DROP} = I_{OUT} R_{ON}$), but we then have to generate a V_{GS} voltage that is higher than the output voltage by at least 3 to 4V, depending on the output current.

To achieve that, this design uses a MAX680, that generate +10V from a +5V input. It supplies a MAX6605 CMOS positive voltage regulator, that drives an N-channel Logic Level FET (RFP25N06L). As the MAX6605 supply current is very low (10 μ A), the drop through the voltage doubler is very low and so the output of the MAX680 is twice the input voltage (10V in the case of a 5V regulator), sufficient to drive the power MOSFET.

The output voltage is set by the feedback resistors R1 and R2

$$V_{OUT} = 1.3V \frac{(R1+R2)}{R1}$$

R3 prevents the MOSFET gate from floating when the regulator is OFF. With a 500mA load, the drop-out voltage is only 100mV, and the quiescent current is typically 1mA, thanks to the CMOS technology of the Maxim's MAX666 and MAX680.

The MAX666 incorporates a low battery detector, whose output (LBO) goes low when the voltage at LBI goes below 1.3V. This may be used to detect pass MOSFET saturation, when V_{IN} is less than $V_{OUT} + 100mV$. This detector may also be used as shown here, to shut down the MAX666 when an overvoltage occurs. When the input voltage will go above the voltage level set by R5 and R6, LBO, tied to the shutdown input SHDN, goes high and shuts down the MAX666 and, prevents excessive dissipation for the pass transistor. R7 provides current to flow through the MAX680 in that case.

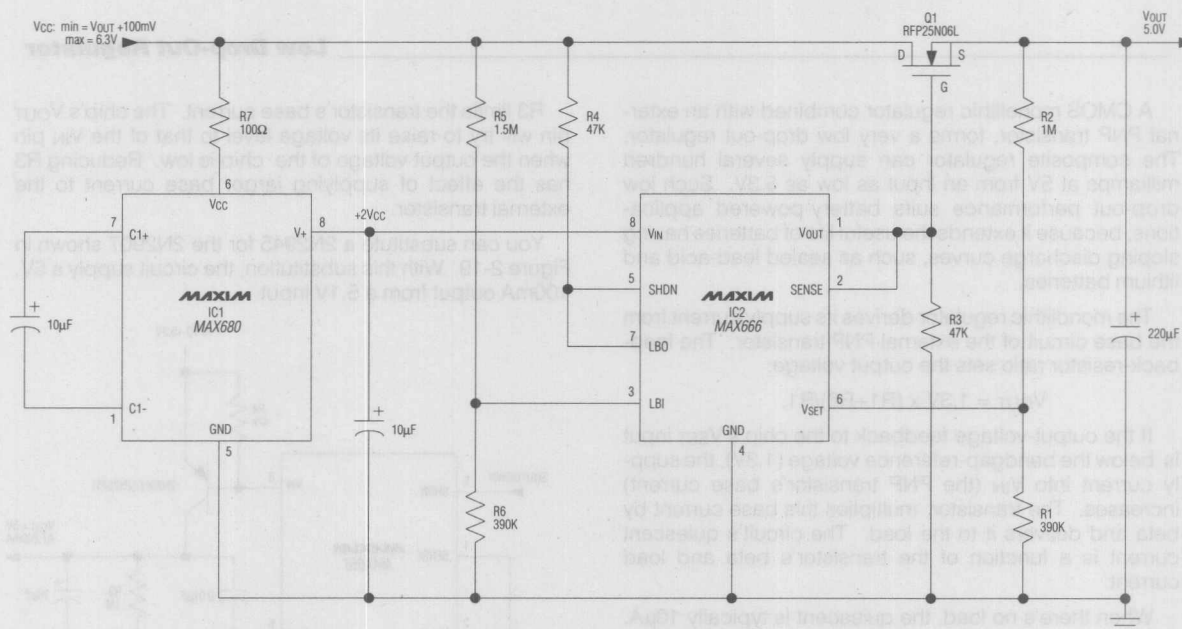


Figure 2-20. A monolithic charge pump doubler IC1 generates a voltage high enough to efficiently drive a power MOSFET Q1, used as the pass element in an ultra-low dropout positive voltage regulator.

When the unregulated DC input voltage falls below 6.0V, the Power Fail Warning signal goes high. The 7805 will continue to supply +5V for a short period of time, drawing its power from the 4700 μ F filter capacitor. This gives the μ P time to save data in CMOS RAM or EEPROM and to perform an orderly system shutdown. Since the 7805 will deliver a 5V output until its input voltage falls to 7.3V, the 7805 will provide 1A for at least 3.5ms.

When the 5V output falls below 4.5V, the Reset or Write Enable output from the ICL7665 goes low. This signal can be used to reset the μ P on power-up, or to gate off the Write and Chip Enable signals to EEPROM and CMOS RAM during power-down.

The ICL7665A OUT2 is set to trip when the 5V output has decayed to 3.9V. This output can be used to prevent the microprocessor from writing spurious data to a CMOS memory, or can be used to activate a battery backup system.

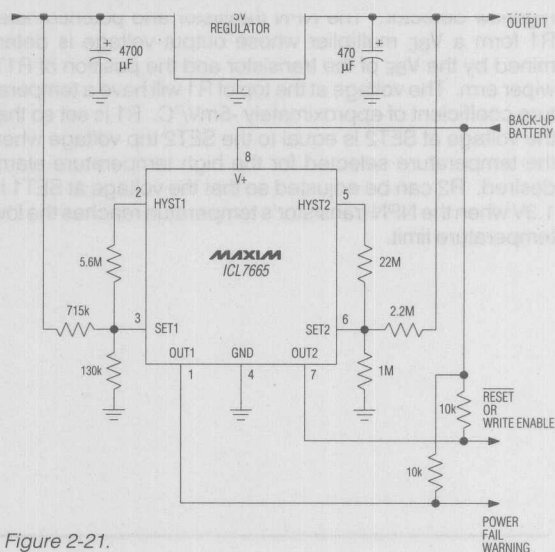


Figure 2-21.

AC Power Fall and Brownout Detector

By monitoring the secondary of the transformer, this circuit performs AC power failure warning. With a normal 110VAC input to the transformer, OUT1 will discharge C1 every 16.7ms when the peak transformer secondary voltage exceeds 10.2V. When the 110VAC power line voltage is either interrupted or reduced so that the peak voltage is less than 10.2V, C1 will be charged through R1. OUT2, the Power Fail Warning output, goes high when the voltage on C1 reaches 1.3V. The time constant $R1 \times C1$ determines the delay time before the Power Fail Warning signal is activated, in this case 42ms or 2 1/2 line cycles. Optional components R2, R3 and Q1 add hysteresis by increasing the peak secondary voltage required to discharge C1 once the Power Fail Warning is active.

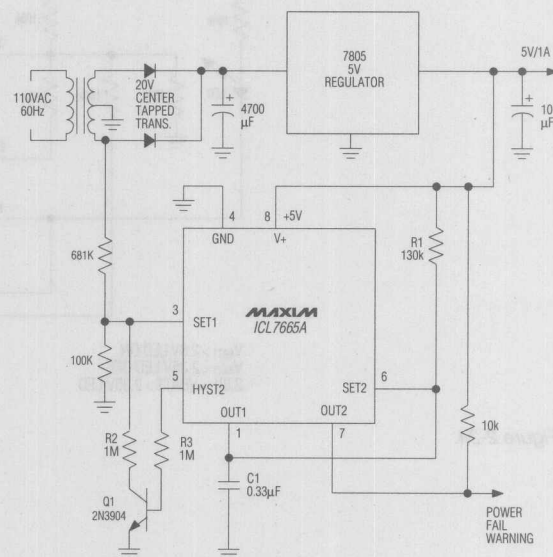


Figure 2-22.

Simple High/Low Temperature Alarm

A simple high/low temperature alarm uses a low cost NPN transistor as the sensor and an ICL7665 as the high/low detector. The NPN transistor and potentiometer R1 form a V_{BE} multiplier whose output voltage is determined by the V_{BE} of the transistor and the position of R1's wiper arm. The voltage at the top of R1 will have a temperature coefficient of approximately $-5\text{mV}/^\circ\text{C}$. R1 is set so that the voltage at SET2 is equal to the SET2 trip voltage when the temperature selected for the high temperature alarm desired. R2 can be adjusted so that the voltage at SET1 is 1.3V when the NPN transistor's temperature reaches the low temperature limit.

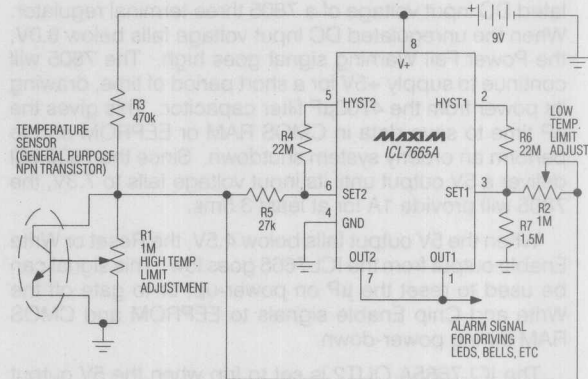


Figure 2-23.

3 State Battery Indicator

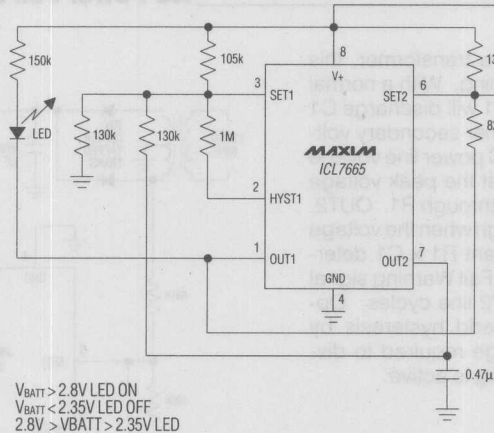


Figure 2-24.

This circuit performs two functions: switching the power supply of a CMOS memory to a backup battery when the line-powered supply is turned off, and lighting a low-battery-warning LED when the backup battery is nearly discharged. The PNP transistor, Q1, connects the line-powered +5V to the CMOS memory whenever the line-powered +5V supply voltage is greater than 3.5V. The voltage drop across Q1 will only be a couple of hundred mV since it will be saturated. Whenever the input voltage falls below 3.5V, OUT1 goes high, turns off Q1 and connects the 3V lithium cell to the CMOS memory.

The second voltage detector of the ICL7665 monitors the voltage of the lithium cell. If the battery voltage falls below 2.6V, OUT2 goes low and the low-battery-warning LED turns on (assuming that the +5V is present, of course).

Another possible use for the second section of the ICL7665 is the detection of the input voltage falling below 4.5V. This signal could then be used to prevent the microprocessor from writing spurious data to the CMOS memory while its power supply voltage is outside its guaranteed operating range.

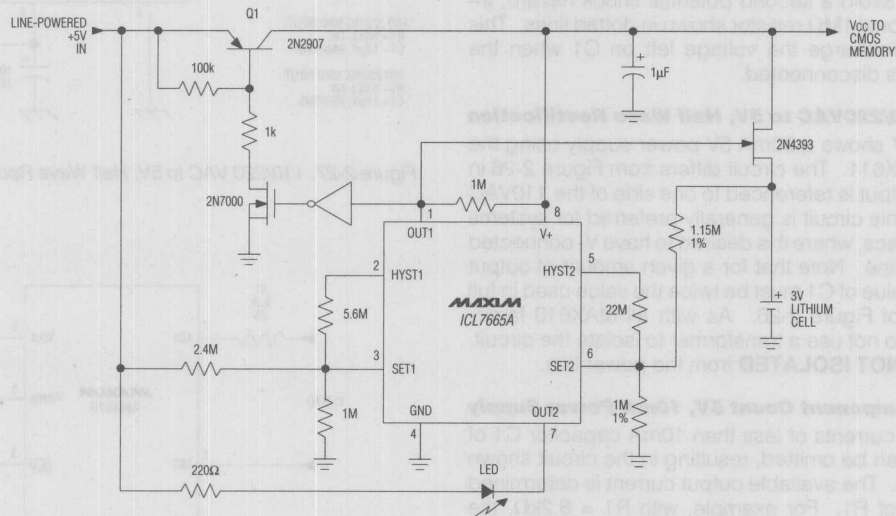


Figure 2-25. Battery Switchover Circuit

Simple Line-Powered 5V Supply

Figure 2-26 shows a 50mA, 5V power supply using the full wave MAX610. Typical component values for both 110VAC and 220VAC 50/60Hz operation are shown. If less than 50mA of output current is needed, the value of C1 can be reduced. For 5V at 35mA from a 110VAC input, C1 = 1 μ F. If only 15mA is needed then 0.47 μ F will suffice. The MAX610/611/612 will not reliably supply more than 50mA.

The output of this power supply is **NOT ISOLATED** from the power line: **the MAX610 and any equipment powered by the MAX610 must be enclosed to avoid shock hazards.** To avoid a second potential shock hazard, include the optional 1M Ω resistor shown in dotted lines. This resistor will discharge the voltage left on C1 when the 110/220VAC is disconnected.

110/220VAC to 5V, Half Wave Rectification

Figure 2-27 shows a 50mA 5V power supply using the half wave MAX611. The circuit differs from Figure 2-26 in that the 5V output is referenced to one side of the 110VAC power line. This circuit is generally preferred for systems that control triacs, where it is desired to have V- connected to the power line. Note that for a given amount of output current, the value of C1 must be twice the value used in full wave circuit of Figure 2-26. As with all MAX610 family circuits that do not use a transformer to isolate the circuit, this circuit is **NOT ISOLATED** from the power line.

Minimum Component Count 5V, 10mA Power Supply

For output currents of less than 10mA capacitor C1 of Figure 2-26 can be omitted, resulting in the circuit shown in Figure 2-28. The available output current is determined by the value of R1. For example, with R1 = 8.2k Ω , the available output current is 10mA, while the power dissipation in R1 is 1.3W. Double both the resistance value and the wattage rating of R1 for use with 220VAC input.

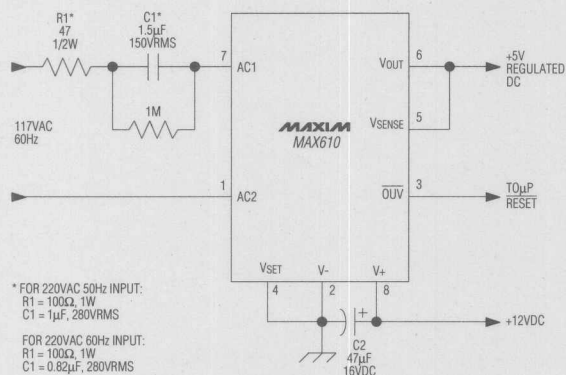


Figure 2-26. Simple Line-Powered 5V Supply

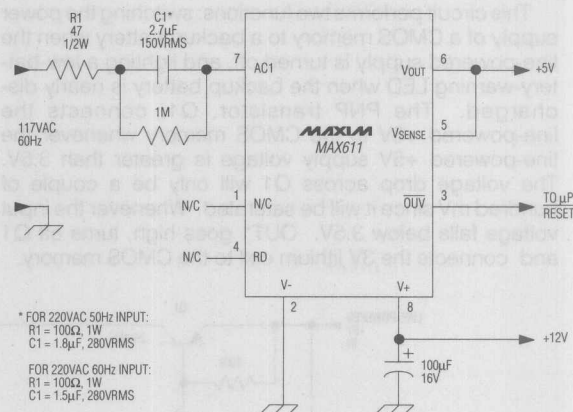


Figure 2-27. 110/220 VAC to 5V, Half Wave Rectification

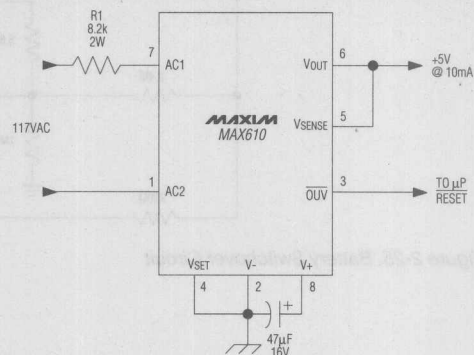


Figure 2-28. Minimum Component Count 5V, 10mA Supply

removed the NiCad battery will supply current through diode D1, and MAX610 output will remain a constant 5V. The MAX610 will continue to deliver 5V out until V^+ is approximately 5.8V and the battery voltage is approximately 6.5V. Alkaline 9V or NiCad 8.4V batteries are also suitable; R2 should not be used with the non-rechargeable 9V alkaline battery.

Polarity Insensitive Battery Powered Supply

Figure 2-30 shows a +5V power supply which will work even if the battery is installed backwards: the full wave bridge rectifier of the MAX612 is well suited for battery powered circuits since its quiescent current is only 70 μ A. The MAX610 can also be used if the battery voltage is less than 10V.

Battery Charger

The +6.7V open circuit or float voltage of Figure 2-31 is set by R2 and R3; the maximum charging current of 60mA is set by the value of C1. Since, unlike transformer driven battery chargers, C1 conducts current throughout most of each line cycle, the ratio of the RMS charging current to the average charging current is only about 1.2:1, and capacitor C2 is optional.

$$I_{AVG(MAX)} = V_{IN} \times 5.56 f_{IN} \times C \text{ (maximum charging current)}$$

f_{IN} = Input Frequency

$I_{RMS} = 1.2 I_{AVG}$; without C2

$I_{RMS} = I_{AVG}$; with C2

The half wave MAX611 can also be used in this circuit, but the value of C1 must be doubled and the ratio of RMS current to average current increases to about 1.7:1.

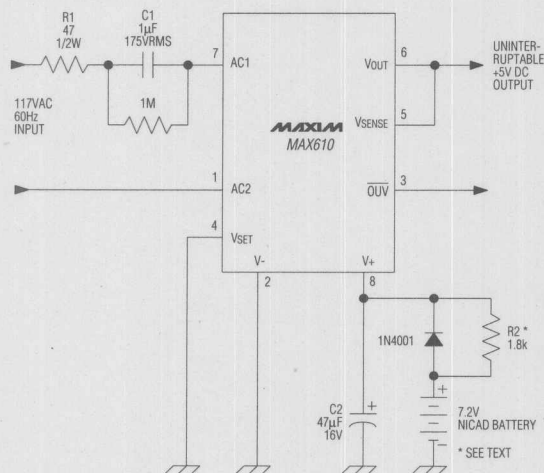


Figure 2-29. Uninterruptable 5V Power Supply

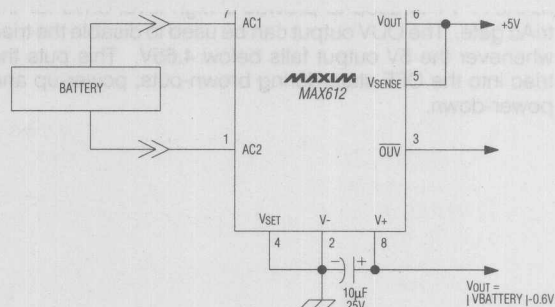


Figure 2-30. Polarity Insensitive Battery-Powered Supply

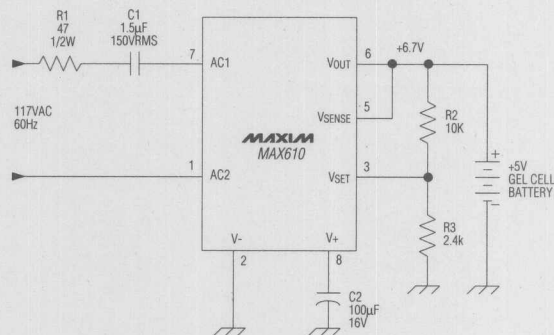


Figure 2-31. Simple Battery Charger

Triac Control Powered From MAX611

Note that V- is tied to the same point as one side of the power line and the MT1 of the triac. The 12V output at the MAX611 V+ is used to provide a high level drive for the triAc gate. The 12V output at the triAc gate. The OUV output can be used to disable the triac whenever the 5V output falls below 4.65V. This puts the triac into the OFF state during brown-outs, power-up and power-down.

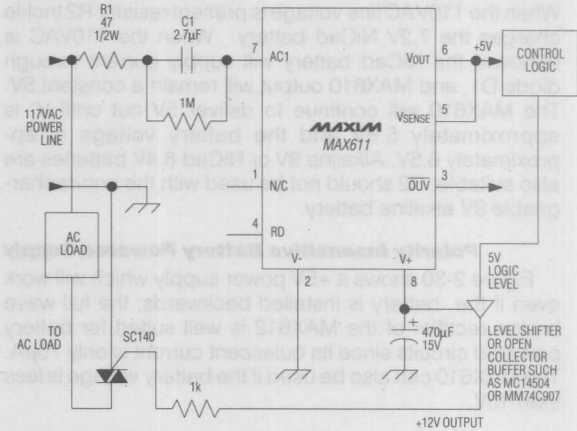


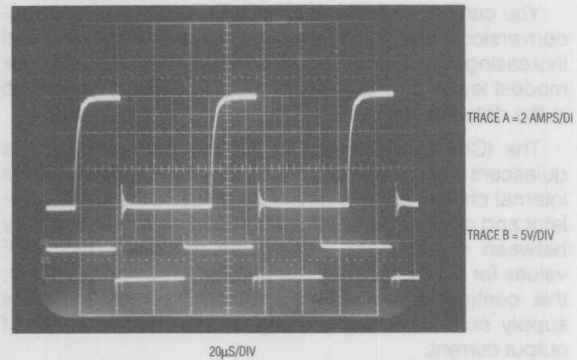
Figure 2-32.

This power switching circuit can be built into a handy piece of portable lab gear for testing power devices and equipment. It can be used to generate an on/off switching signal to test load transient response times, transformer characteristics, or to control small DC motors or similar loads. A power N-channel MOSFET is controlled by an external logic signal such as a function generator; when the input is at a logic "high", the MOSFET is ON and has a resistance of less than 0.1Ω .

Optical isolation, provided by a common 4N26 optocoupler, allows the MOSFET source to be tied to a voltage other than ground. The degree of isolation will be determined by transformer winding insulation in the power supply, which is rated at 500V (the optocoupler has an order of magnitude higher rating). Isolation gives nearly complete flexibility for DC loads; as long as the MOSFET D-S and D-G voltage ratings are observed, one can have a $\pm 500V$ difference between the logic input and MOSFET outputs.

Switching speeds are shown in the photo; with 6 Amps of load current, the output will respond in less than $20\mu S$. Faster response can be realized by using a high speed optocoupler (for example: an HP6N138), and by adding collector base anti-saturation clamps (schottky diodes) to the input inverter transistor and phototransistor.

The pulser was built in a 2.5" by 5" by 4" enclosure using isolated BNC and banana jacks for I/O connections.



TRACE A = LOAD CURRENT
TRACE B = LOGIC INPUT

Figure 2-33.

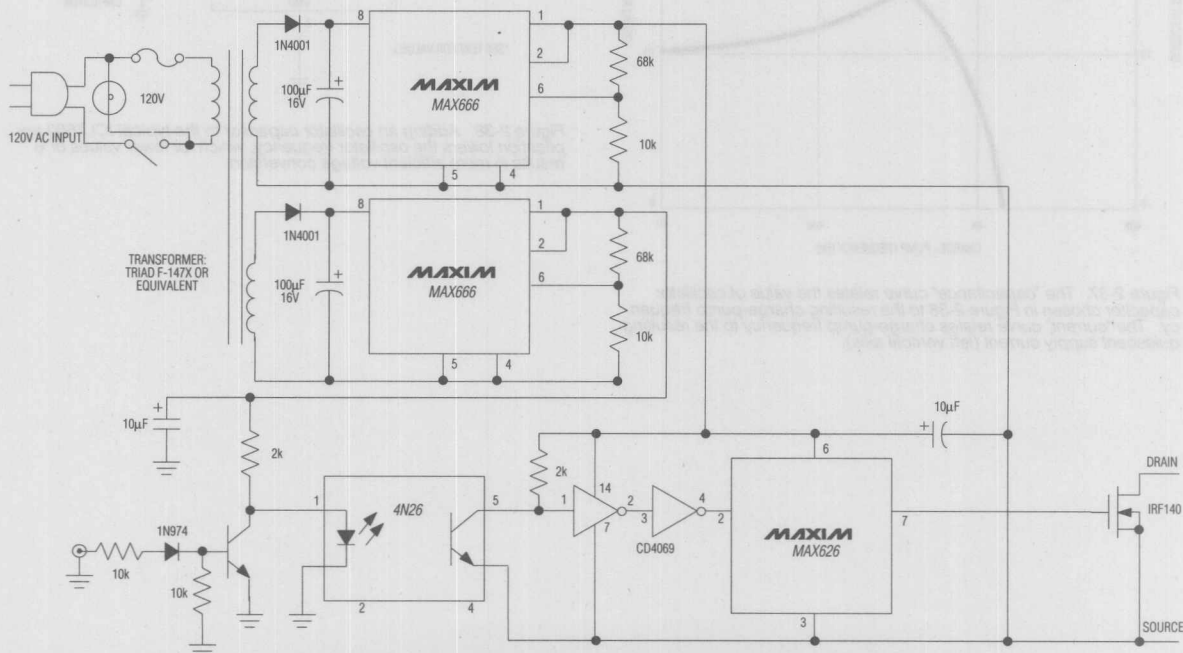


Figure 2-34.

You can improve the efficiency of an ICL7660 voltage-conversion circuit by lowering the oscillator frequency and increasing the external capacitor values. Though useful for modest levels of I_0 , this technique is not clearly described in the data sheet.

The ICL7660's conversion efficiency depends on its quiescent supply current, which in turn depends on the internal charge pump's drive frequency. The chip's oscillator and divide-by-two circuit normally sets the frequency between 4 and 5kHz. Using the recommended 10 μ F values for the flying capacitor and the reservoir capacitor, this configuration consumes about 70 μ A of quiescent supply current while providing a conservative 20mA of output current.

Increasing the frequency by overriding the oscillator with an externally applied signal causes a proportional increase in the quiescent current. Or, connecting an external oscillator capacitor to pin 7 (Figure 2-38) slows the oscillator,

causing supply current to approach a minimum value of about 10 μ A at 40Hz (Figure 2-37).

Slowing the oscillator improves the efficiency, but to avoid a corresponding increase in the output ripple voltage you must also make an inversely proportional change in the values of the external flying capacitor and reservoir capacitor. For example, setting the oscillator to 400Hz by connecting 100pF to pin 7 requires 100 μ F for the flying and reservoir capacitor. Such an arrangement still provides 20mA of output current but consumes only one fifth the quiescent current (15 μ A).

Note that you can reduce the capacitor values if lower I_0 is allowed. Setting the oscillator to 40Hz, for example, (by connecting 1000pF to pin 7) provides the highest efficiency possible. Leaving the flying and reservoir capacitors at 100 μ F gives a maximum low of 2mA, a no-load quiescent current of 10 μ A, and a power conversion efficiency of 98%.

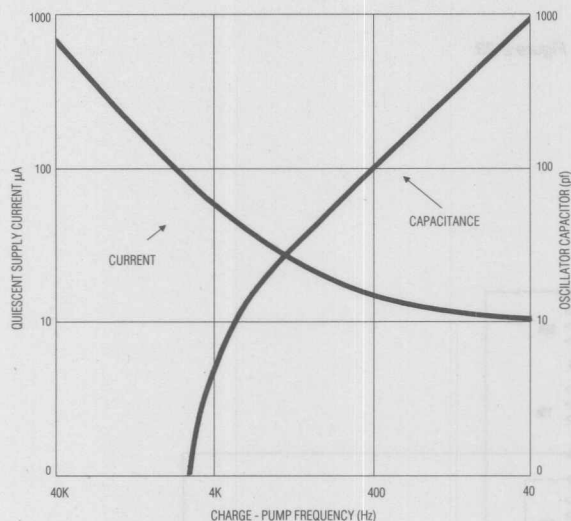


Figure 2-37. The "capacitance" curve relates the value of oscillator capacitor chosen in Figure 2-38 to the resulting charge-pump frequency. The "current" curve relates charge-pump frequency to the resulting quiescent supply current (left vertical axis).

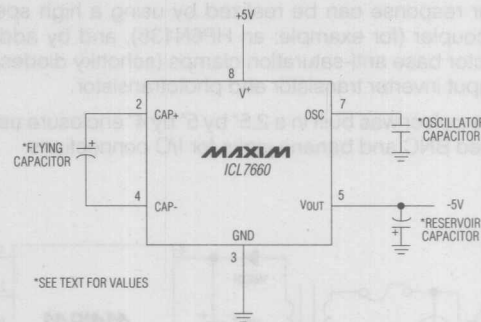
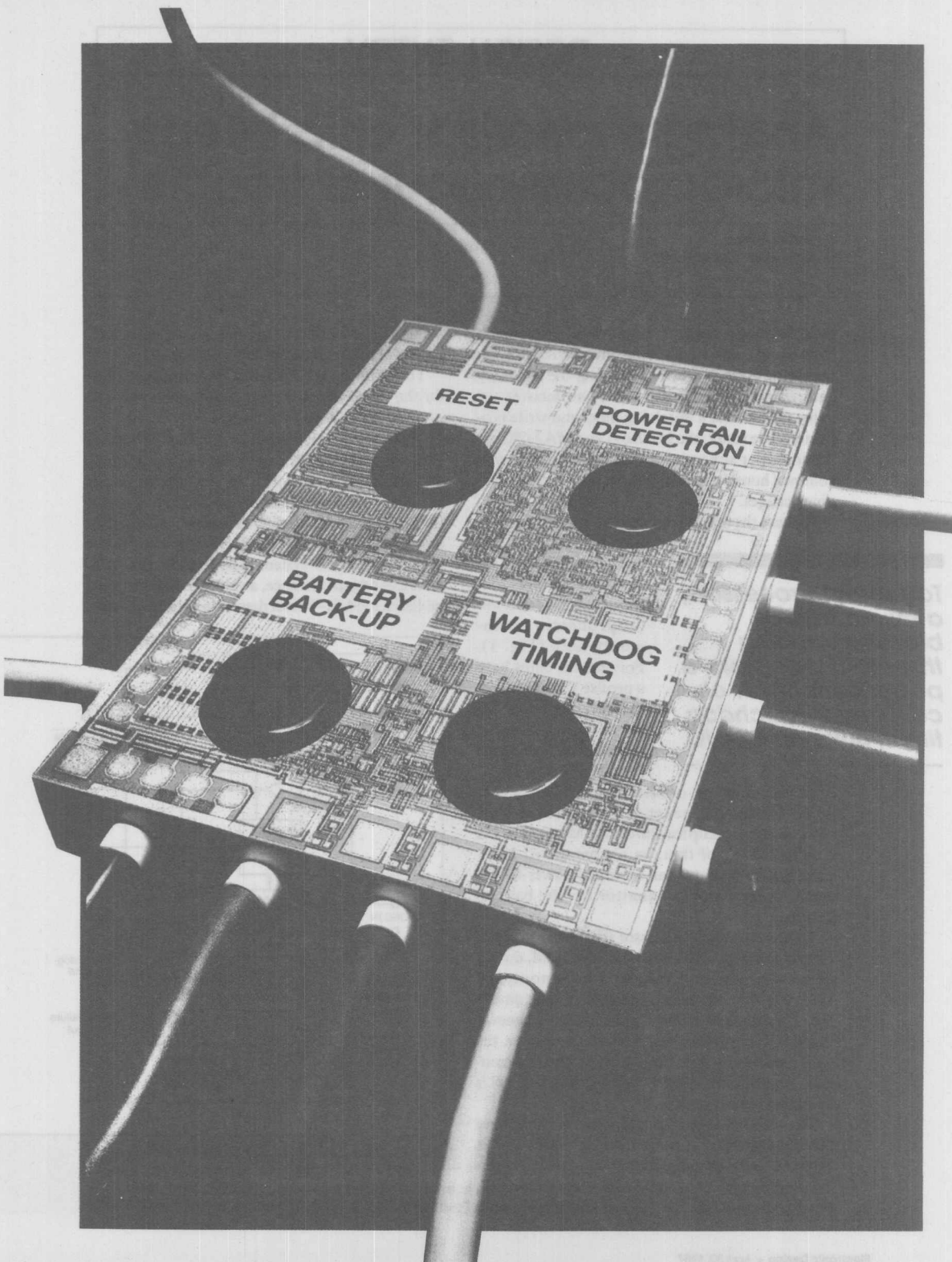


Figure 2-38. Adding an oscillator capacitor to the typical ICL7660 application lowers the oscillator frequency, which for lower values of I_0 results in more efficient voltage conversion.



Analog supervisor chip keeps microprocessor out of trouble

Charlie Allen
Maxim Integrated Products

Goal: to sharply reduce the complexity, component count, and space of standard microprocessor supervisory circuits while improving the accuracy and reliability of reset and battery-switchover circuits. Add to that a watchdog timer and write protection. The result: the MAX691 and MAX690 microprocessor supervisory ICs, which pack many common housekeeping functions into 16-pin and 8-pin packages.

Because the needs of microprocessor systems defined the ICs, the supervisory circuits contain several seemingly distinct functions that microprocessors commonly need (Fig. 1). For one, the chips have a precise 4.65-V threshold detector and a 50-ms timer that generate an accurate reset signal for any power-up, power-

To protect processors, a mixed bag of blocks, including threshold detectors, a power-switchover circuit, and a watchdog timer, unite on one IC.

er-down, brownout, or momentary-interrupt condition. For another, power-switchover circuitry offers a battery backup for CMOS RAMs or real-time clocks. On top of that, an uncommitted 1.3-V threshold comparator can serve as a power-failure warning indicator or monitor for the backup battery.

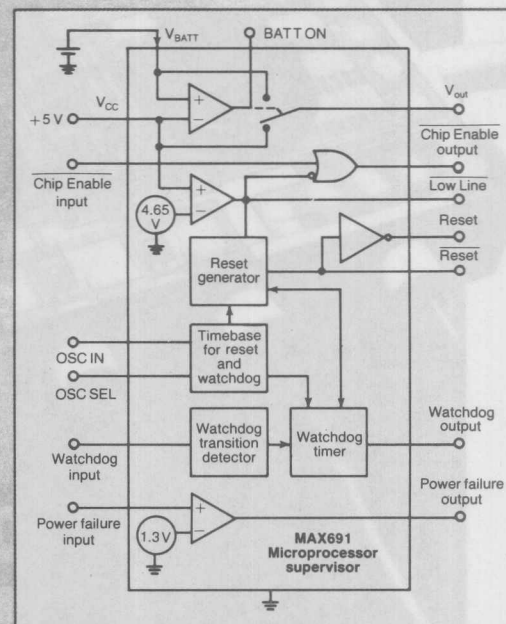
To keep the microprocessor from writing incorrect data into a CMOS RAM or EEPROM, during power-up, power-down, or a brownout, the MAX691 has chip-enabling circuitry. The circuit forces a Chip Select output enable high whenever the +5-V supply falls below 4.65 V. Moreover, the chip's watchdog timer monitors software execution, resetting the microprocessor if execution is disrupted for any reason.

The reset and watchdog time-out periods have three pin-selectable timing options. The first is based on an on-chip oscillator and needs no external components. The second uses an external clock. Finally, the designer can choose the minimum reset

pulse width and watchdog time-out period by tuning the oscillator with one external capacitor.

The eight-pin MAX690 has fewer timing options for the watchdog timer and reset-pulse width and no chip-enable gating circuitry.

The reset function relies on a reference-voltage technique with much more reliability than simple RC circuits, which work well if a change occurs abruptly between completely off and +5 V. But if the power is slowly applied or lost, or if a brownout or momentary loss occurs, the RC circuit does not properly reset the system. The reset section contains a bandgap reference, a voltage divider that establishes the 4.65-V reset detection threshold, and a



1. The basic functions provided by Maxim's MAX691 microprocessor supervisory IC are battery back-up for V_{CC}, reset pulses, and watchdog timing to ensure proper operation.

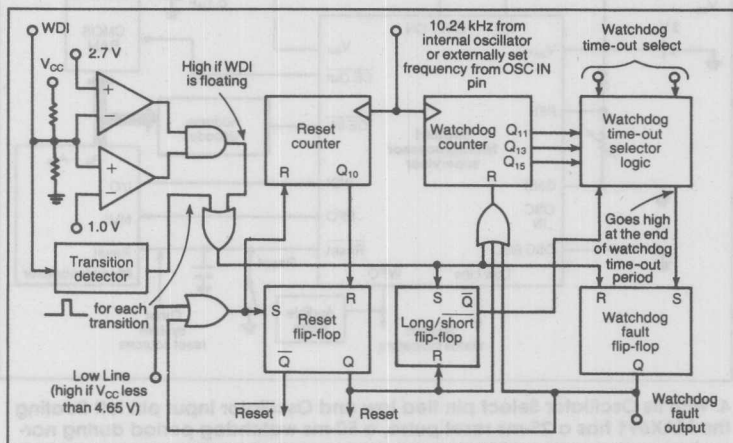
50-ms retrIGGERABLE monostable oscillator.

The voltage detector forces the Reset output low when ever the +5-V V_{CC} input drops below 4.5 V. The circuit holds Reset low until the supply stays above 4.75 V for 50 ms, ensuring that the microprocessor receives the minimum reset pulse width specified by the manufacturer. The designer can extend this pulse width by adding a capacitor to the oscillator input pin or shorten it by overdriving the oscillator input. The voltage detector also serves a second purpose: forcing the Chip Enable output high whenever the +5-V input is incorrect.

Although the 4.65-V threshold is a nominal value, the 4.5-V minimum and 4.75-V maximum are guaranteed because the thresholds are trimmed at the wafer level. Trimming involves fusible metal links like those on bipolar PROMs. A Low Line output offers an instantaneous view of the voltage-detector status. The Reset output, however, goes high only after the input voltage has been at a valid level for 50 ms.

The Reset pin offers a "weak output," which works as an active CMOS output driving high or low or as a wired-OR output when connected to open-collector outputs. The pin can also supply the pullup current needed by the open-collector outputs connected to the bus. This dual capability is possible because the pin is a CMOS output but with only a limited source-current capacity.

When connected to a high-impedance input, the weak output drives with full CMOS output swings of ground to V_{CC} . But when connected to an open-collector or wired-OR bus, the limited source-current output lets the weak output be pulled down by any device with a sink current of only 10 μ A. Another benefit is the output's guaranteed minimum 1- μ A pullup current, which eliminates the need for an external pullup resistor on a wired-OR bus.



2. The chip's watchdog circuitry looks for periodic strobes from the program. If no strobe is received in the allotted time, the Watchdog Fault Output, WDO, goes high, and Reset issues a 50-ms reset pulse.

The battery-switchover circuitry, although shown in the block diagram as merely an SPDT switch, is more complicated than that. In practice, a voltage comparator checks V_{CC} against the battery voltage. As long as the supply is higher than the battery, V_{CC} connects to the output terminal, V_{out} . The connection, however, is through a pnp transistor whose base-drive modulation circuitry saturates the transistor while minimizing base current.

SHORT-CIRCUIT PROTECTION TOO

When V_{CC} falls to within 100 mV of the battery voltage, the circuit turns off the base drive, and a 400- Ω MOS switch connects the battery to V_{out} . With the MOS switch the voltage drop is about 4 mV, compared to about 500 mV across the diode switch used in a discrete circuit typically found in battery-backup circuits. The base-drive circuitry includes a thermal-shutdown circuit that reduces base drive if the junction temperature is too high, thereby lending short-circuit protection to V_{out} .

With V_{CC} present, battery current is a maximum of ± 1 μ A and typically is a 10-nA charging current. This level extends battery life while remaining within the allowable charge current of even the smallest lithium batteries.

When V_{CC} falls to about 700 mV below battery voltage, a second comparator shuts down all circuitry not needed in the battery-backup mode. In this low-quiescent-current state, the typical draw on the battery is about 600 nA, ensuring a long battery life.

The chip's Battery On pin, which has a sink current of 5 mA, indicates whether V_{CC} or the battery is powering V_{out} . It can directly drive the base of an external pnp transistor if the battery-backed power bus needs more than 50 mA of output current during normal operation.

An internal pnp transistor, meanwhile, is guaranteed

to have a maximum voltage drop of 300 mV at 50 mA, a level that will run several CMOS RAMs if their Chip Enable inputs function to reduce the average current. A 0.1- μ F bypass capacitor at the output supplies the high-current spikes the RAMs draw for a few nanoseconds during each access cycle.

Besides working with batteries, the chip's power-switchover circuitry supplies short-term power backup with standard capacitors or the new farad-size units.

The third major section of the chip is the watchdog timer, a function often desired but seldom found (see

ing. When that input floats, two internal resistors bias it at an invalid logic level detected by internal voltage comparators (Fig. 2).

On the job, the microprocessor drives the WDI pin with an I/O line that is periodically strobed. At each strobe, the supervisory chip resets the timer. If the microprocessor fails to strobe WDI for the programmed time period, a watchdog fault occurs. Typical reasons for a failure to strobe include hardware problems, a temporary disruption caused by voltage transients, and software errors that put the microprocessor in an endless loop.

ALARM ACTIVATED

If a watchdog fault occurs, the chip sends a 50-ms reset pulse and the Watchdog Fault Output, WFO, goes low. The output remains low, and the chip periodically pulses the Reset line until WDI is again strobed. For the greatest reliability, the Watchdog Fault output can activate an alarm and trigger hardware that places the equipment controlled by the microprocessor into a fail-safe mode.

The designer can set the time-out period in several ways. One of two internally preset time delays can be selected with a logic level on the Oscillator Input pin while the Oscillator Select pin is high. Slow-response systems, such as instruments that update displays, usually can tolerate errors for several seconds. In this type of system, the nominal 1.6-s watchdog time-out suffices.

On the other hand, an airplane autopilot or a programmable controller must quickly reset after a malfunction. Such systems usually need a 100-ms or faster time-out period. Since most systems have special power-up routines that run after a reset, the chip waits up to 1.6 s for them, even if the 100-ms time-out period is chosen.

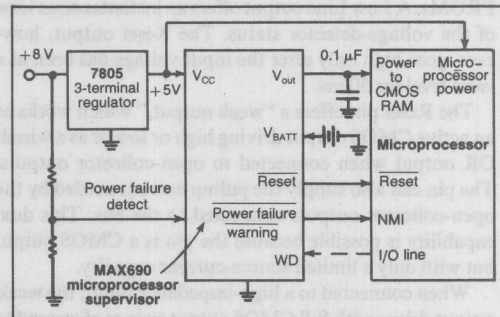
A designer has two ways to externally set the exact time-out period. One way is to overdrive the Oscillator Input pin with an external clock. Because the watchdog timer is an oscillator and a counter rather than the RC monostable circuit, a 200-ns pulse can reset the timer. The designer can then use a decoded Write signal to drive WDI.

The alternative is to select

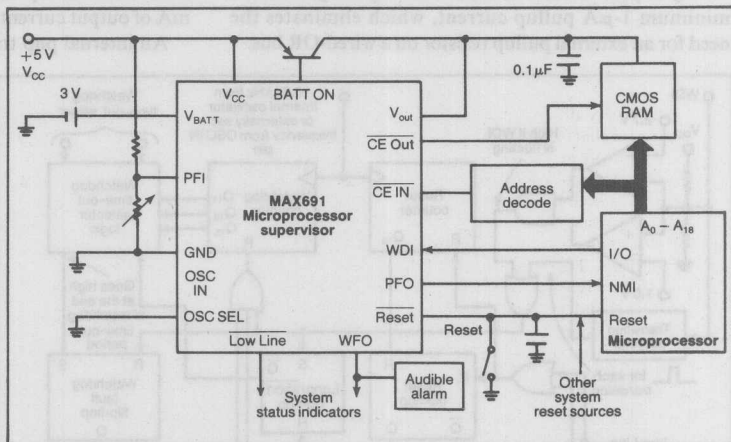
ing capacitance to the Oscillator Input reduces its frequency and stretches the time-out period. For example, a 2-nF capacitance lengthens the time-out to 10 s.

Typically, the MAX690 monitors V_{CC} for a one-board controller system and generates a 50-ms reset pulse when needed (Fig. 3). An +8-V dc source fed to the 7805 three-terminal regulator is scaled by two external resistors and applied to the chip's Power Fail Warning detector, which has a 1.3-V threshold.

As a result, when the raw dc falls below 8 V, the supervisory chip's Power Fail Output goes low, interrupting the microprocessor through its nonmaskable interrupt



3. In a circuit with a three-terminal voltage regulator, the MAX690—a simplified version of the 691—sends a power-failure warning to the microprocessor as soon as the raw 8-V dc begins to drop.



4. With its Oscillator Select pin tied low and Oscillator Input pin left floating the MAX691 has a 25-ms reset pulse, a 50-ms watchdog period during normal operation, and a 200-ms watchdog period after any reset.

(NMI). If the voltage continues to fall, the regulator's 5-V output will begin to drop. When it reaches 4.65 V, the supervisory chip asserts Reset, halting the microprocessor and preventing further access to the RAM. As V_{CC} approaches the battery voltage, the chip replaces V_{CC} with the battery at V_{out} , ensuring continued power to the CMOS RAM. When V_{CC} falls to 700 mV below the battery, the chip shuts down all of its own unneeded circuitry, reducing its current drain to 600 nA.

RAM POWER RESTORED

When the dc voltage begins to build up again, the sequence reverses, except that Reset stays low for 50 ms after V_{CC} rises above 4.65 V. When 5 V is again present, V_{out} restores power to the RAM, guaranteeing a maximum voltage drop of 300 mV between V_{CC} and V_{out} at an average 50-mA current.

A more sophisticated system based on the MAX691 has the Battery On output driving an external transistor to increase power on the battery-backed bus to 250 mA (Fig. 4). Also, the Watchdog Fault Output sounds an external alarm if recovery from a malfunction is impossible. In this system, if V_{CC} is at an invalid level, the Chip Enable gating circuit blocks write cycles to the CMOS RAM or real-time clock, preventing the microprocessor from corrupting the data in the RAM during power-up, power-down, or a brownout.

Tying Oscillator Select low and leaving Oscillator Input floating reduces the reset time-out to 25 ms. This configuration also sets the watchdog time-out to 50 ms during normal operations and 200 ms immediately after a reset.

The reset bus contains a manual switch and a 0.1- μ F capacitor that make possible manual system resets. This circuit contains a simple method of generating a power-failure warning, needing only the +5-V input and two resistors. The resistors set up a warning threshold of 4.8 V. The processor has only the time it takes V_{CC} to drop from 4.8 to 4.65 V to save any data into RAM.

Because all the sections of the MAX690 and 691 are independent, any unnecessary functions can be ignored. For example, a designer who does not want battery back-up and power-failure warning can eliminate the battery and the two resistors and connect the battery and Power Failure Inputs to ground. If the watchdog timer is not desired, the Watchdog Input is left floating. □

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Watchdog on guard

Nearly every designer has operated equipment that can lock up, needing a reset to restore normal operation. The watchdog circuit's job is to detect such malfunctions and to automatically issue reset commands.

Performance of this task can take many forms. The most sophisticated is a separately executing microprocessor that independently calculates results and compares them with the master computer's actions. At the lower end are schemes that demand, within a specified time, a response to an interrupt issued by the watchdog circuit. In between are circuits that issue a pseudorandom number or bit

stream that the microprocessor must match to avoid a fault indication.

The most common watchdog circuit, though, checks the microcomputer's operation by monitoring an I/O line that is toggled under program control. This scheme assumes that if the processor periodically toggles the I/O line properly, then it is correctly executing the program. Such a circuit can tell if the microprocessor is stuck in a loop so long as the loop does not toggle the I/O line.

A watchdog circuit needs software, the simplest being a few lines of code that toggle the I/O line. The code must be in a section of software that

executes frequently enough that the time between toggles is less than the watchdog time-out period. Typically, the watchdog software is in the system or supervisory software, either in a section that responds to a periodic interrupt or in the section that executes when the system is idle.

Another common software technique controls the I/O line from two sections of the program. The software might set the I/O line high while operating in the foreground mode and set it low while in the background or an interrupt mode. Then both modes must execute correctly or else the watchdog timer issues a reset pulse.

DESIGN IDEAS

EDITED BY CHARLES H SMALL

Transistor powers low-dropout regulator

James E Dekis

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The monolithic regulator chip in Fig 1, combined with an external pnp transistor, forms a very-low-dropout regulator. The composite regulator can supply several hundred milliamps at 5V from an input as low as 5.3V. Such low-dropout performance suits battery-powered applications, because it extends the useful life of batteries having sloping discharge curves, such as sealed lead-acid and lithium batteries.

The monolithic regulator derives its supply current from the base circuit of the external pnp transistor. The feedback-resistor ratio sets the output voltage:

$$V_{OUT}=1.3V \times (R_1+R_2)/R_1.$$

If the output-voltage feedback to the chip's V_{SET} input is below the bandgap-reference voltage (1.3V), the supply current into V_{IN} (the pnp transistor's base current) increases. The transistor multiplies this base current by β and delivers it to the load. The circuit's quiescent current is a function of the transistor's β and load current.

When there's no load, the quiescent current is typically 10 μ A. For larger load currents, the quiescent current is simply the load current divided by the transistor's β . The regulator chip can sink 40 mA max. When you enable the chip's shut-down input, the circuit consumes 6 μ A typ. R_4 supplies current to the chip under no-load conditions.

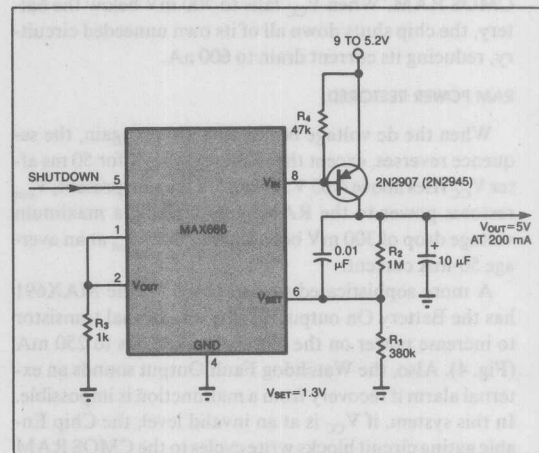


Fig 1—A monolithic regulator chip driving a dummy load sets the base current of an external, series-pass pnp transistor; the result is a very-low-dropout regulator for batteries whose output voltage droops under load.

R_3 can limit the transistor's base current. The chip's V_{OUT} pin will try to raise its voltage level to that of the V_{IN} pin when the output voltage of the chip is low. Reducing R_3 has the effect of supplying larger base currents to the external transistor.

You can substitute a 2N2945 for the 2N2907 shown in Fig 1. With this substitution, the circuit will supply a 5V, 100-mA max output from a 5.1V input. **EDN**

EDN

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What follows is a discussion of some basic data acquisition topics in question and answer form. Its intent is to aid those who have not had recent experience with analog-to-digital and digital-to-analog conversion designs. The terms

"A/D" and "ADC" are frequently used for "analog-to-digital converter", while "D/A" and "DAC" are used for "digital-to-analog converter".

How significant is analog-to-digital converter type when considering different A/Ds? How do they compare?

Manufacturers typically don't provide details on internal IC operation in applications literature unless the A/D in question uses some exotic conversion technique. Although specifications alone are usually enough to define the A/D or D/A you need for a particular application, an awareness of the strengths of different IC designs can be very helpful, at least from the standpoint of picking a performance range. A/Ds fall primarily into three categories: successive approximation, integrating, and flash types.

Successive Approximation The most commonly encountered type of ADC is that employing a successive-approximation register (SAR). SAR designs have from 8- to 12-bit resolution and operate at a wide range of speeds from 10 to 100 μ s. Conversion is accomplished by stepping through a sequence of trial-and-error comparisons between the unknown input signal and a series of binary-weighted reference levels. The result of each successive comparison serves to narrow the range of reference level used for the subsequent comparison.

A block diagram of a typical SAR ADC is shown in Fig. 3-1. The 12-bit device contains a 12-bit DAC, control logic, and output latches. Conversion is performed by comparing the unknown analog voltage with the DAC output. When this matches the unknown voltage, conversion is complete and the digital number corresponding to the analog voltage is presented at the output.

The number of bits of resolution provided by the converter is equivalent to the number of comparisons made. The primary advantages of this technique are that (1) only one comparator is needed for the conversion and (2) higher resolution does not greatly increase the conversion time.

For example, a 10-bit ADC will only be ten-eighths slower than an 8-bit device of the same basic type because only two additional comparisons are needed to obtain 4

times the resolution. The binary nature of the SAR search also makes the converter ideal for interfacing to computers and microprocessors.

Unfortunately, the SAR converter requires a large number of steps to complete an approximation routine and therefore is susceptible to error if the analog input changes in the middle of the SAR search. For this reason, noise rejection usually is not high. For certain inputs, a sample-and-hold stage or filter may be needed to stabilize the input signal while AD conversion is under way.

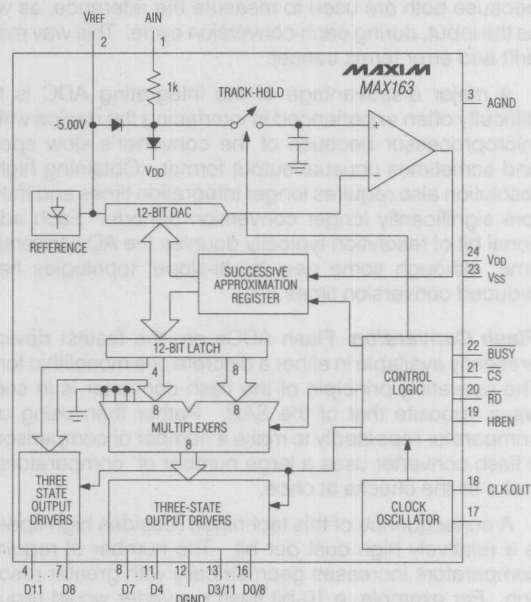


Figure 3-1. Successive Approximation Register (SAR) analog-to-digital converter (ADC) with on-chip track-and-hold.

Integrating Conversion Integrating ADCs, including single-, dual-, and multi-slope designs, are most commonly found in digital meters and instrumentation systems. They are relatively slow, but this is usually not a problem because the results are used primarily for visual readout. The strong point of an integrating ADC is high resolution, offering as many as 20 bits of digital data (6 decimal digits). Low-cost monolithic converters of this type commonly handle ± 2000 counts, which is equivalent to 12 bits.

The most popular type of integrating converter is the *dual-slope design*, in which the unknown signal ramps the input of an integrator up from 0V for a time set by a fixed number of clock cycles. A reference voltage of opposite polarity then discharges the integrator and returns it to zero. The discharge time, which is proportional to the input voltage, is measured by counting the number of clock pulses (Fig. 3-2).

The dual-slope integrating ADC, by nature, has high noise rejection because the output represents the average value of the input signal over the integration time. This circuit is able to ignore changes in its integrator and clock because both are used to measure the reference, as well as the input, during each conversion cycle. This way many drift and error terms cancel.

A major disadvantage of the integrating ADC is the difficulty often experienced in interfacing the device with a microprocessor because of the converter's slow speed and sometimes unusual output format. Obtaining higher resolution also requires longer integration times and therefore significantly longer conversion periods. Each additional bit of resolution typically doubles the AD conversion time, although some new "multi-slope" topologies have reduced conversion times.

Flash Conversion Flash ADCs are the fastest devices presently available in either a discrete or a monolithic form. The operating principle of the flash converter is in some ways opposite that of the SAR. Rather than using one comparator repeatedly to make a number of comparisons, a flash converter uses a large number of comparators to make all the checks at once.

A consequence of this technique (besides high speed) is a relatively high cost per bit. The number of required comparators increases geometrically with greater resolution. For example, a 10-bit flash converter would require 1023 comparators. For this reason, flash converters are not commonly employed for applications that demand more than 8-bit resolution. They are, however, widely used in high speed 6- and 8-bit applications such as video signal processing.

Some new ADC devices combine flash and SAR techniques to provide high speed without using huge numbers of comparators. One example of this approach is the half-flash ADC, which performs an 8-bit conversion by combining the results of two 4-bit flashes. Figure 3-3 shows the basic concept of the half-flash converter. This principle has been expanded to 10 bits with the MAX151.

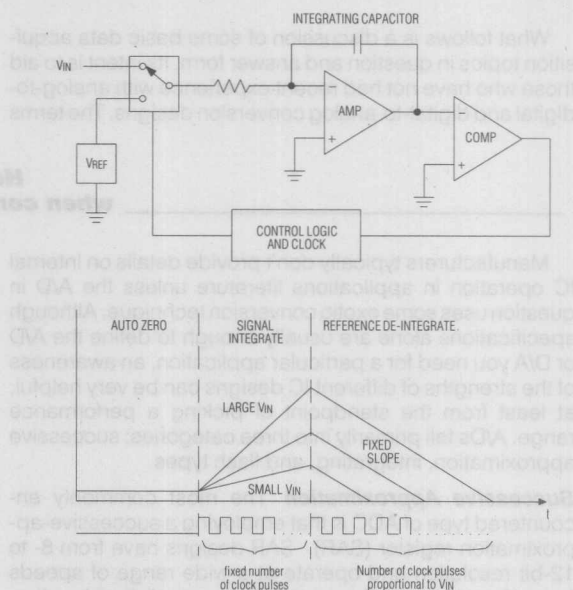


Figure 3-2. Simplified block diagram of dual-slope integrating ADC

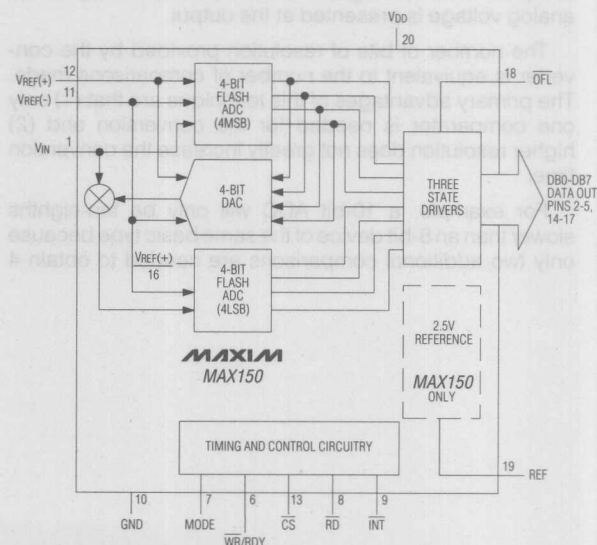


Figure 3-3. Half-flash ADC. This 8-bit converter uses 32 comparators in two 4-bit flash circuits

How does A/D and D/A converter resolution relate to accuracy?

Resolution is the number of segments into which a data converter divides an analog signal. It is quite a bit different from accuracy, which for an A/D is the converter's error in deciding a signal's magnitude. With a D/A, accuracy is the error in generating a specific output voltage or current. Accuracy and resolution USUALLY have comparable magnitudes in a particular converter, but not always. In higher resolution (12 bits and up) devices, 0.025% or greater untrimmed accuracy adds cost to the IC. For example, a low cost 12-bit A/D can resolve a 10 V input range to within 2.5 mV, but more often than not the digital output won't be accurate to that amount without some circuit adjustment.

High accuracy without trimming can of course be had in many data converter products, but usually at significant cost. In many applications, the expense of this initial accuracy is often wasted. If the device is linear, (more on linearity later) its absolute error spec is a moot point if other parts of the system require calibration anyway. A good example of this is the A/D used in supermarket weigh scales. The scale's required accuracy is 0.01 pounds out of 25, which can't be achieved without some type of

calibration because of transducer errors. Since other parts of the circuit need trimming anyway, A/D error can be adjusted as part of the system. In such a case, a less costly A/D, with greater absolute error, does just as well as one with zero gain error. A converter with tighter accuracy only reduces the required trim range, so the extra expense of untrimmed accuracy makes sense only if adjustments are eliminated altogether. This is also true for DACs. One example, the MX7531J D-to-A converter, has 12 bit resolution but only 8 bit accuracy. It provides 12 bit resolution at reduced cost, so if the application requires manual adjustments anyway, the DAC's accuracy compromise doesn't affect performance.

To be complete, it should be also be pointed out that there are some instances where having an accuracy spec that exceeds resolution is also useful. One such instance is when a digital-to-analog converter sets an op amp or some other amplifier's gain. There may be only a small number of settings required (for example, 8 gains equals only 3 bits of resolution), but the accuracy of each set gain might be quite high.

What is the difference between bipolar and CMOS D/A converters?

From an applications standpoint, the semiconductor fabrication process employed in a particular integrated circuit is usually of academic interest only and is not as important as actual specifications and performance. However, in the case of CMOS and bipolar D/A converters, there are some operational differences related to fabrication which warrant attention.

Bipolar D/A converters rely on a process that is much the same as that used for standard linear devices such as

transistors and op amps. The performance depends on matching current sources that can also be switched at high speeds (Figure 3-4). The magnitudes of these current sources are binarily weighted and each is controlled by a digital input bit. The DAC's output current is then the sum of the current sources that have been switched on. A voltage reference, which is occasionally included on chip (as in the MX565), sets the full scale output.

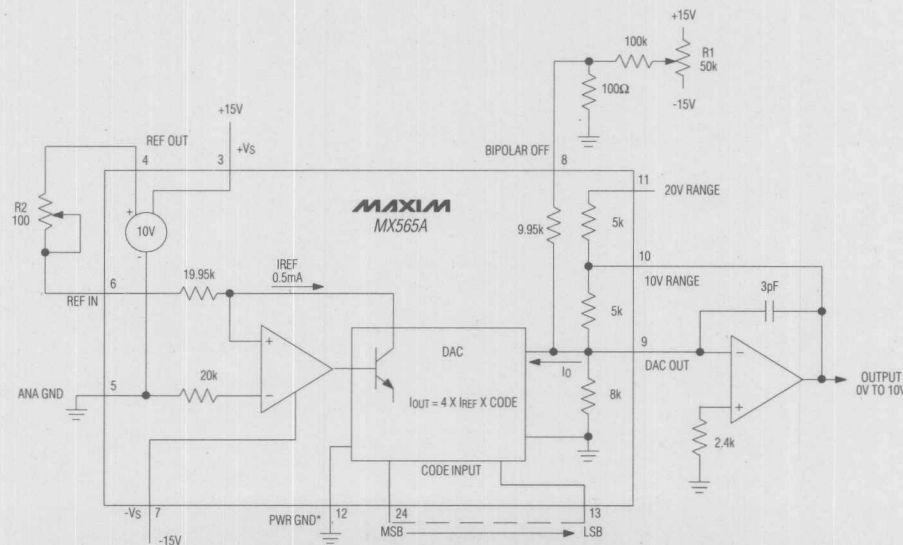


Figure 3-4. 12-bit current-output DAC made with bipolar processing contains active transistor current sources.

CMOS DACs may have either a current or voltage output. Common current-output types, such as the MX7541A, differ from bipolar converters in that they are "passive" in the analog signal path (Figure 3-5). This means that the output is controlled by matched resistors and analog switches rather than active transistor current sources. Excellent on-chip resistor matching provides precision to 14 bits, as with the MX7538, and beyond. Current-output CMOS DACs are often called "multiplying D/A converters" because the reference input accepts a wide variety of signals which are then controlled by the digital input code. Voltage-output CMOS DACs, such as the 8-bit MX7224, have more limited reference flexibility, but are often more convenient to use because they include buffered voltage outputs.

Other advantages of CMOS DACs over bipolar are lower power consumption, single supply operation, and excellent gain stability with temperature. They are also more common in multiple configurations, such as with the MX7228, which has eight voltage-output 8-bit DACs on one chip. A disadvantage of current-output CMOS parts is that their output compliance as current sources is poor because they are not active. This means that output current is linear only when the DAC output is terminated at 0V. Consequently, current-output CMOS DACs nearly always need an output amplifier (Figure 3-6).

Though somewhat less versatile than CMOS, bipolar DACs such as the MX566 are typically faster with better settling characteristics. They sometimes can be used in multiplying applications as well, but only in a limited fashion because reference bandwidth and polarity are often restricted. The active current output on a bipolar DAC has one advantage: in some situations a suitable voltage output can be generated without an op-amp by simply terminating the DAC's current output with a resistor.

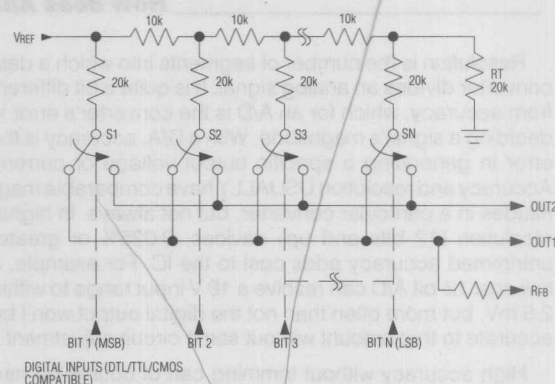


Figure 3-5. A CMOS current-output DAC contains switches and matched resistors.

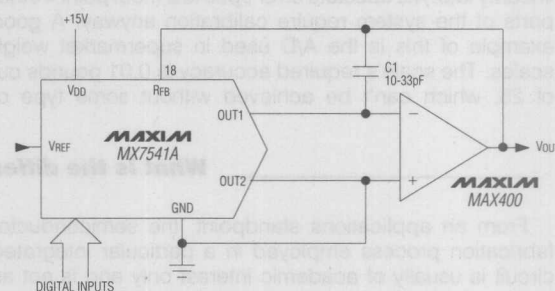


Figure 3-6. A 12-bit CMOS current-output DAC with op amp for voltage output

What can non-linearity (most often referred to as "linearity") specs hide?

How are monotonicity and "no missing codes" determined?

There are several different methods of defining data converter linearity (or non-linearity). Each definition has its own justification, but the result of such variety is confusion. One device can give rise to several different linearity numbers, under a variety of specifications. It pays to be familiar with how a number is generated if it is going to be compared with other specs. Two common ways of qualifying linearity specs are "best straight line fit" and "endpoint fit" (see Figure 3-7).

The best straight line approach makes no claims about zero (offset) error, full-scale errors, or the slope of the transfer function. It simply quantifies, in LSBs or %, the A/D's maximum deviation from a straight line that best approximates the function (i.e. provides the lowest error). The actual location of the ideal line is not defined. This is a "pure" linearity spec since it includes no other errors. It also usually gives the best looking (lowest) number for a given device.

Endpoint fit, on the other hand, uses the actual endpoints of the converter's transfer function (see above section) as the ideal line before measuring deviation. The line's slope and position are not adjusted to minimize the error. The number generated from this technique is usually larger than that derived with the best straight line approach.

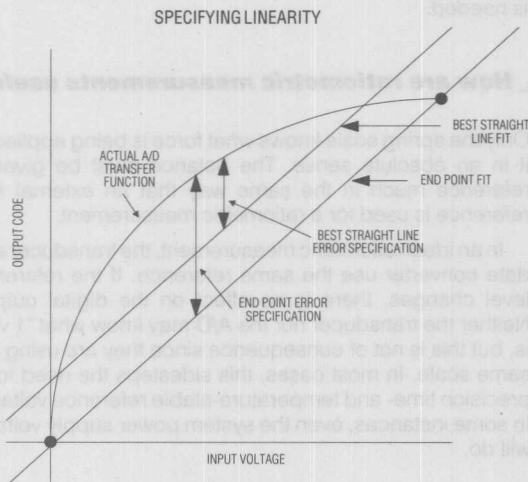


Figure 3-7. "Best Straight Line" and "Endpoint" Linearity produce different specifications for the same A/D

Concern with linearity often hinges on whether a device has "no missing codes" (in the case of an A/D) or is "monotonic" (for DACs). This means that the output of a converter will increase or, at the very least, stay the same as the input increases (Figure 3-8). Manufacturers (including Maxim) often state this as a guaranteed condition ("no missing codes", "guaranteed monotonic") on the data sheet, while others provide a specification called "differential nonlinearity". Some provide both.

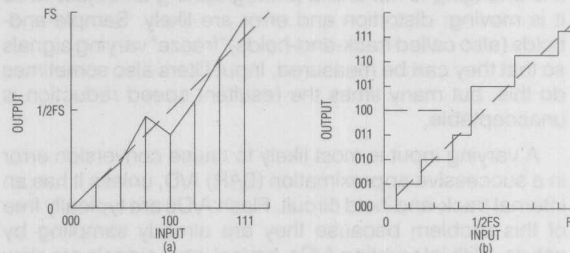


Figure 3-8. Nonmonotonic D/A Converter (a) and A/D Converter with Missing Code (b)

Differential linearity describes the deviation of each analog "step" from its ideal size of 1 LSB (Figure 3-9). A differential nonlinearity (DNL) spec of "0.5 LSB" means that all steps are at least 0.5 LSB and no more than 1.5 LSB. DNL of 1 LSB or less guarantees monotonicity or "no missing codes". It says that all steps are at least 0 LSB and no more than 2 LSB. A step of 0 LSB, though usually not desired, does (barely) satisfy monotonicity requirements.

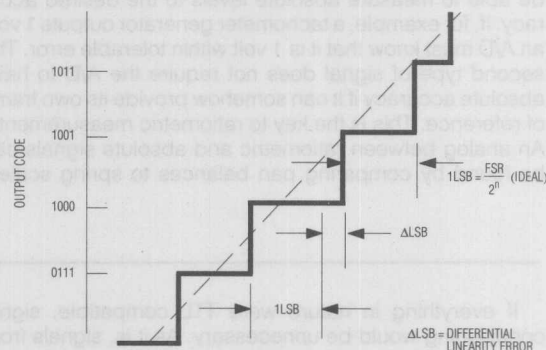


Figure 3-9. Differential Linearity Error

This specification, sometimes referred to as "Absolute Accuracy" lumps all A/D errors (zero error, nonlinearity, reference error, etc.) into one. It is the largest difference between the ideal and actual analog input voltage that results in each output code. A fact that sometimes causes

confusion is that a range of input voltages and not just one specific voltage, produces a given output code. For this reason the "ideal" input voltage for a code is defined as the midpoint of the voltage range for that code.

When are sample-and-holds needed in data acquisition?**What are the consequences of not using them?**

In many measurement applications, you have no control over the speed of an input signal. Measuring a signal while it is changing is not unlike photographing an object while it is moving: distortion and error are likely. Sample-and-holds (also called track-and-holds) "freeze" varying signals so that they can be measured. Input filters also sometimes do this, but many times the resultant speed reduction is unacceptable.

A varying input is most likely to cause conversion error in a successive approximation (SAR) A/D, unless it has an internal track-and-hold circuit. Flash A/Ds are typically free of this problem because they are already sampling by nature. With integrating A/Ds, typical input signals are slow enough to not be a problem. Without the benefit of a sample-and-hold, input changes are simply averaged over the A/D integration time. This produces no "catastrophic" errors for transient input signals. In fact, it is often desirable

for noise rejection purposes. Sampling is only needed with integrating A/Ds if the instantaneous value of the input, rather than an average value, is required.

In an SAR A/D, it is assumed that the input will not change by more than 1/2 LSB during an entire conversion cycle. Since each "guess" in an SAR search tells the A/D converter what its next step will be, an input shift in the middle of the comparison sequence can play havoc with the conversion process. When this happens, all that is known for sure is that the digital output lies between the minimum and maximum values that the input had during the conversion. These bounds are not very helpful if large input transients occur at inopportune times. The output will neither represent the input's average value nor will it represent the value at any predictable time. A sample-hold, or an A/D with an internal sample-hold such as the MAX163, is needed.

How are ratiometric measurements useful?

When measuring physical quantities, the signals of interest are either absolute voltages which correspond to a physical quantity, or they are in the form of a varying impedance or ratio which must be externally driven to obtain a signal. The first type of signal requires that the A/D be able to measure absolute levels to the desired accuracy. If, for example, a tachometer generator outputs 1 volt, an A/D must know that it is 1 volt within tolerable error. The second type of signal does not require the A/D to have absolute accuracy if it can somehow provide its own frame of reference. This is the key to ratiometric measurements. An analog between ratiometric and absolute signals can be found by comparing pan balances to spring scales.

Only the spring scale knows what force is being applied to it in an absolute sense. The balance must be given a reference much in the same way that an external A/D reference is used for a ratiometric measurement.

In an ideal ratiometric measurement, the transducer and data converter use the same reference. If the reference level changes, there is no effect on the digital output. Neither the transducer nor the A/D may know what "1 volt" is, but this is not of consequence since they are using the same scale. In most cases, this sidesteps the need for a precision time- and temperature-stable reference voltage. In some instances, even the system power supply voltage will do.

How are differential inputs used?

If everything in nature were TTL compatible, signal conditioning would be unnecessary. As it is, signals from various analog sources are often not conveniently created with respect to the measuring system's ground. Such signals frequently arrive with large offsets or common mode noise which need to be removed. In other cases, the difference, and not the absolute magnitude of two quantities may be of interest, as with differential pressure or temperature.

In all these cases, analog electronics can be added to make the differential measurement. Having it incorporated into the A/D converter, however, reduces parts count and improves reliability. Differential inputs provide a means of canceling noise or offsets common to both input lines. The device responds only to the difference between signals on its plus and minus inputs, and rejects common-mode signals that appear on both pins.

What is the difference between an op-amp and an instrumentation amp?

You should choose an instrumentation amplifier when differential inputs are not available on a selected A/D, and the difference function is still needed. An instrumentation amp is not simply a high performance op amp. Devices referred to as such are actually mislabeled. An instrumentation amplifier is a differential input device with high impedance inputs and either a fixed or adjustable stable gain than can be conveniently set with one or two resistors.

Although an op-amp is a differential input device, precise differential closed-loop gain can't be set without four

closely matched resistors. Though this configuration is often used, it can't be easily adjusted and has fairly low-impedance inputs. Instrumentation amps are widely used to amplify low level differential signals such as those generated by pressure transducers, weight sensors (strain gauges), many temperature sensors and devices which rely on low level bridges for linear output. Many of these types of signals are too low level to be converted by an A/D directly.

When is signal isolation necessary?

In signal conditioning, input isolation is the next giant step beyond differential inputs. It is used where the signal to be measured is not or cannot be electrically connected to the data acquisition system in any way. This is widely done in medical electronics and in industrial environments where the input may be "hot" to an AC power line, either inadvertently or by design. Also, isolation is gaining wider use in low-level data acquisitions where the common-mode signals may not be high, but where it nevertheless is useful as a means of avoiding ground loops and noise pickup. This is especially true in large systems where many signals from remote locations are returned to one point. Each

return line is likely to be at a slightly different potential, and the possibility of interference and/or damage could exist without individual channel isolation.

In many applications, there is no need to convert back to analog form if an A/D conversion will be the end result anyway. In these cases, considerable expense can be saved by the use of serial output A/D or V/F converters. The outputs of these devices can easily be isolated with small transformers or optical isolators and can then be read in digital form. Serial output devices work especially well because only one data line needs to be isolated. (See Figure 3-10).

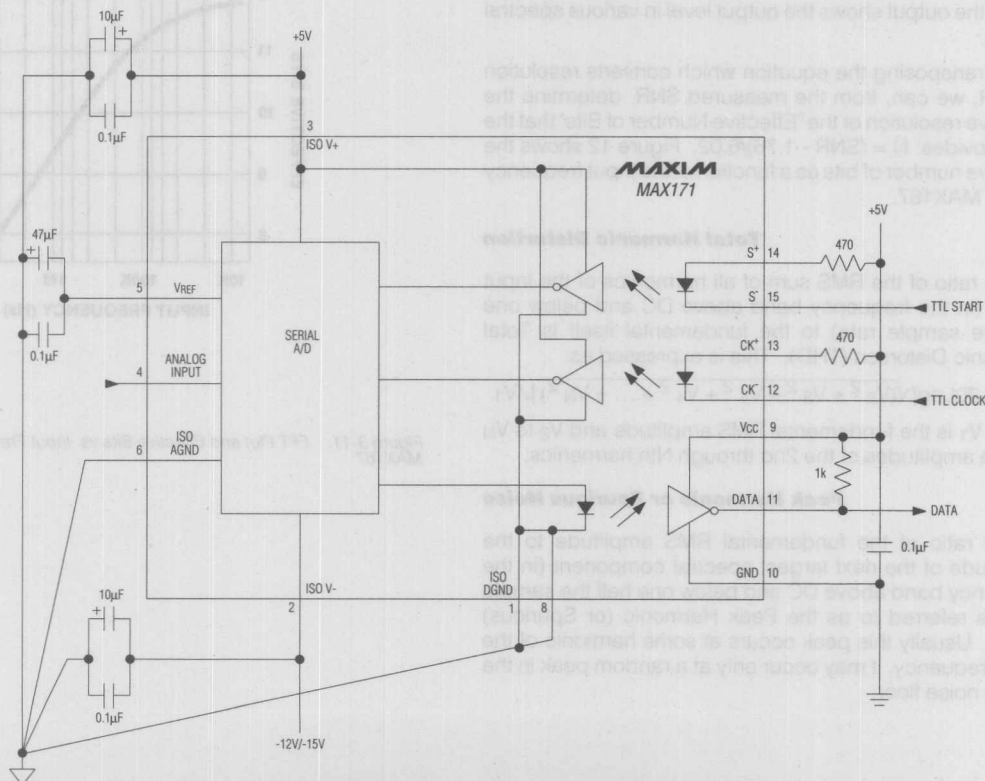


Figure 3-10. The MAX171 simplifies analog isolation by combining a 12-bit serial A/D and opto-couplers in one package

specifications such as Zero and Full Scale Error, Integral Non-linearity (INL), and Differential Non-linearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals but are less useful in signal processing applications where the A/D's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so other tests, as described below, are required.

Signal-to-Noise Ratio and Effective Number of Bits

The ratio of the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the Signal-to-Noise Ratio (SNR). The A/D output band is limited to frequencies above DC and below one half the A/D sample (conversion) rate. This usually (but not always) includes distortion as well as noise components. For this reason the ratio is sometimes referred to as "Signal-to-Noise + Distortion".

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the A/D's resolution: $SNR = (6.02N + 1.76)dB$, where N is the number of bits of resolution. A perfect 12-bit A/D can, therefore, do no better than 74dB. Figure 3-11 shows the result of sampling a pure 10kHz sinewave at a 100kHz rate with the MAX167. An FFT plot of the output shows the output level in various spectral bands.

By transposing the equation which converts resolution to SNR, we can, from the measured SNR, determine the effective resolution or the "Effective Number of Bits" that the A/D provides: $N = (SNR - 1.76)/6.02$. Figure 12 shows the effective number of bits as a function of the input frequency for the MAX167.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one half the sample rate) to the fundamental itself is Total Harmonic Distortion (THD). This is expressed as:

$$THD = 20\log[\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}]/V_1$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Peak Harmonic or Spurious Noise

The ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one half the sample rate) is referred to as the Peak Harmonic (or Spurious) Noise. Usually this peak occurs at some harmonic of the input frequency, it may occur only at a random peak in the ADC's noise floor.

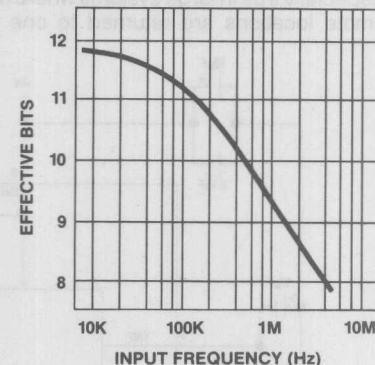
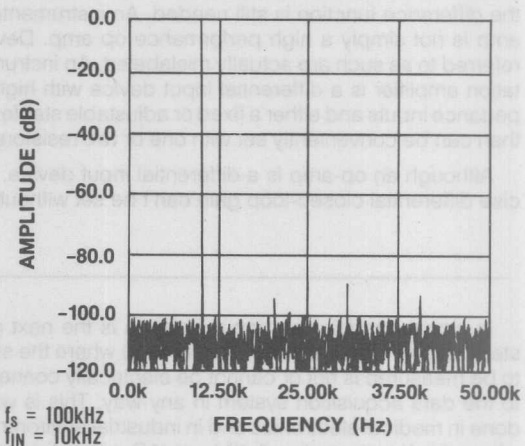


Figure 3-11. FFT Plot and Effective Bits vs. Input Frequency for MAX167

This is a tough one. The greatest problem facing a data acquisition design is that it must eventually enter the "real world". "Device failure, poor accuracy, doesn't meet spec" and other oft stated maladies are, more often than not, a direct result of some type of disregard for basic electromagnetic principles and Ohm's Law. Experience has shown that solutions for these types of problems often range from compensating oscilloscope probes to properly bypassing power supplies. What follows are some tips and suggestions.

First, if in doubt about grounding procedure, use single-point grounding to prevent ground loops (which can generate unwanted currents when cut by invading magnetic fields). Applying this grounding philosophy also keeps voltage drops in high current lines from affecting the ground points of more sensitive circuits. The use of simpler "chain" grounding will not stop this type of feed-back which can cause DC errors and/or oscillation. Separate analog and digital supplies are desirable for precision measurements, however with A/Ds and D/As that have both analog and digital ground pins, it is best to connect BOTH chip ground pins to only the analog ground. Ideally, the analog and digital circuitry should be completely isolated, but cost often prohibits this. An effective cost compromise is to filter a portion of the system supply with a separate RC network, and use that supply only for analog and A/D circuitry.

In most cases, careful consideration should be given before cutting corners on grounding and supply bypassing, especially if there are plans for expanding the system. An important goal is to protect analog circuitry from transients or power supply shifts caused by digital logic transients. Shields, if used, should be "water tight" and thought of as an extension of the instrument or system enclosure. Shielded cables should be grounded at one end only, preferably at the single-point-ground.

Analog signals should be amplified to their highest practical level or digitized as soon as possible. It is not wise to run a low-level signal across a circuit board past clock lines, relays, switching circuits, etc... only to amplify both the signal and acquired noise before entering an A/D. Noise is best minimized by amplifying immediately and digitizing the signal at the source if possible. Serial output A/D converters work well for this when the signal source is remotely located. It's also wise to physically separate analog and digital circuitry. Use separate circuit areas on the PC board, or separate boards if possible. In extreme cases, a completely separate shielded sub-enclosure may be required for analog circuits if very low level signals are involved.

When troubleshooting and debugging analog data acquisition hardware, never give blind trust to emulators, development systems, and so forth. These digital instruments can be invaluable time savers, but be sure to verify the results by other means when what they say conflicts with common sense. Since these devices provide "second-hand" information about the state of your hardware, it is not uncommon to be fooled by the very problem that is being chased. There is really no substitute for observation right at the pins of suspect devices. Once the approximate location of a problem has been found, it is always most effective to clear away as many interface/buffer/reality-obscuring layers as possible. Blame should be reserved until it can be proven by direct observation, a.k.a. an oscilloscope.

A good text which takes much of the "witchcraft" out of grounding and other practical analog problems is "Grounding and Shielding Techniques in Instrumentation", by Ralph Morrison, published by Wiley and Sons, New York, NY. Although relatively small, it gives a complete discussion of this area without cumbersome levels of math.

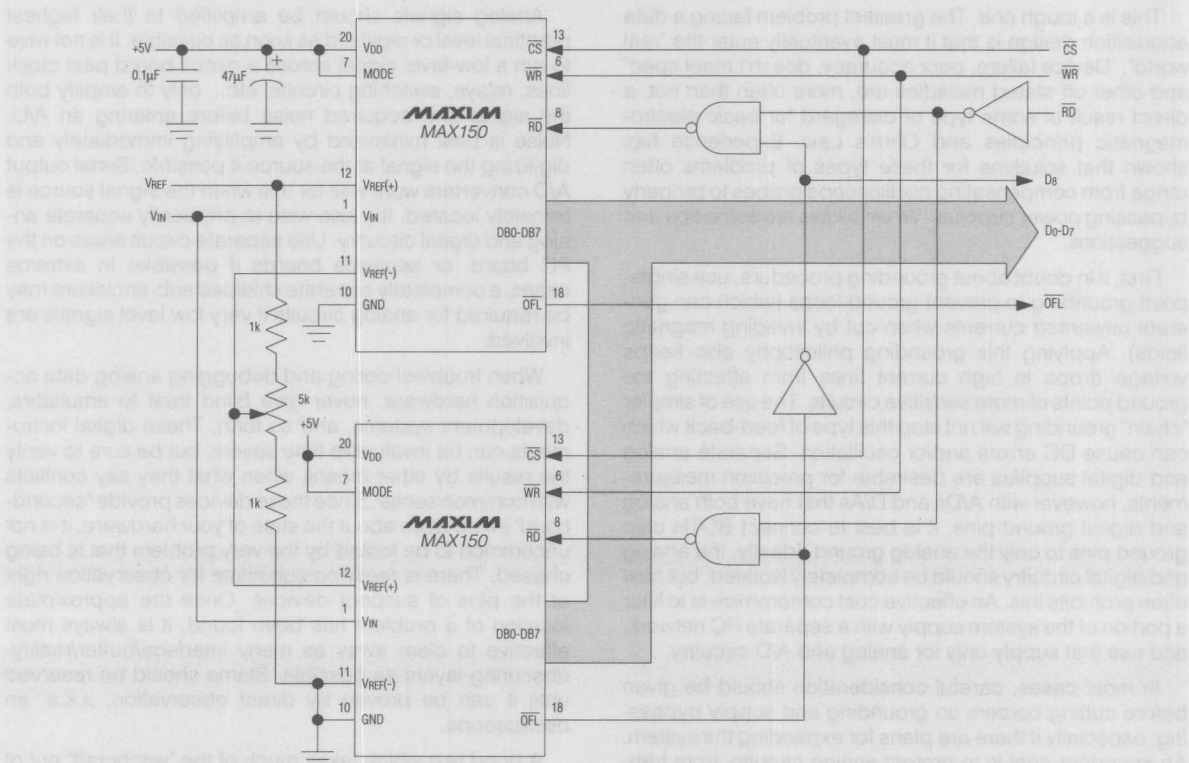


Figure 3-12.

Fast Sample and Infinite-Hold

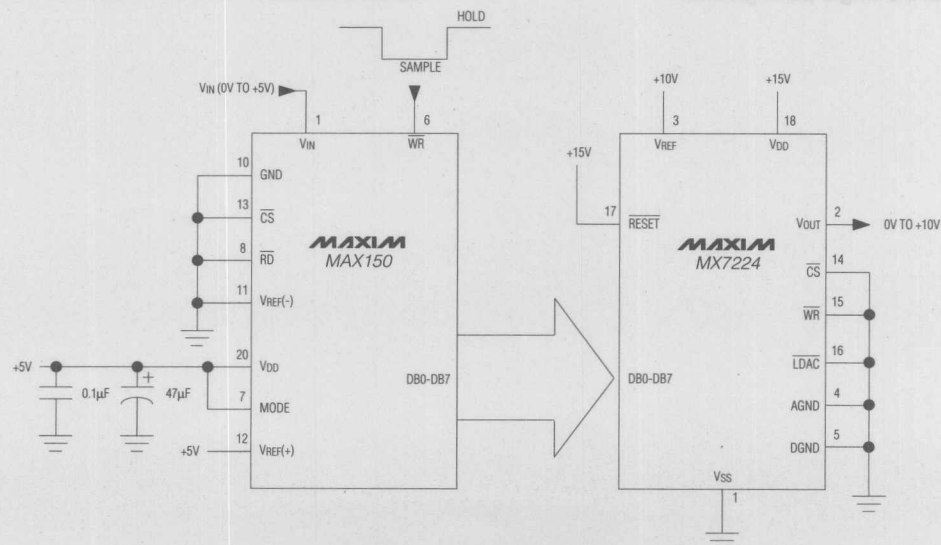
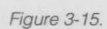
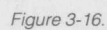


Figure 3-13.

Telecom A/D Converter





This sample-and-hold holds its acquired input for an infinite amount of time with no droop. It also has excellent input bandwidth, aperture delay, and aperture jitter. A MAX163 sampling ADC samples the input voltage. The input signal is held on the falling edge of the hold signal, which goes to the RD pin of the MAX163. The hold signal must be at least 8.5µsec wide. This initiates a conversion on the MAX163. After 8µsec, the conversion result is updated on the outputs of the ADC. These outputs are fed to the digital inputs of a DAC (Maxim MX7545). Since the hold signal was low throughout the conversion, the DAC updates its output as soon as the MAX163 data is available. Therefore, the output of the DAC is a re-construction of the original input signal. On the rising edge of the hold signal, this data is latched into the DAC, and the ADC becomes ready to sample another signal.

The requirement that the hold signal be low during the conversion simplifies the ADC-DAC interface, and allows data to be transferred between the two chips without "glue" logic. A MAX400 amplifier converts the current output of the DAC into a voltage. The DAC also uses the internal reference output of the MAX163 as its reference input. This reference conveniently has the correct polarity, so that a 0-5V input to the MAX163 is reconstructed correctly by the MX7545. The internal reference also eliminates one source of mismatch in the reconstruction of the input signal.

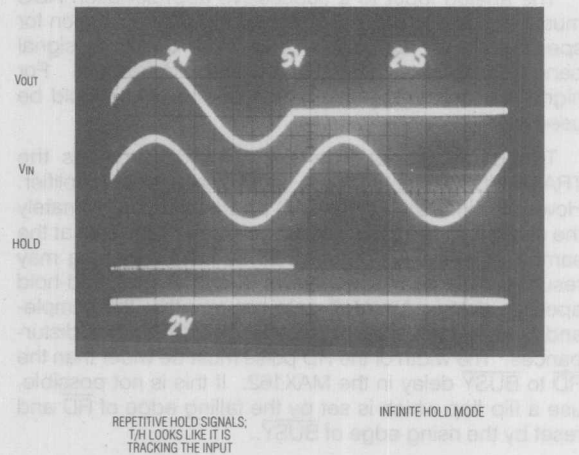


Figure 3-17.

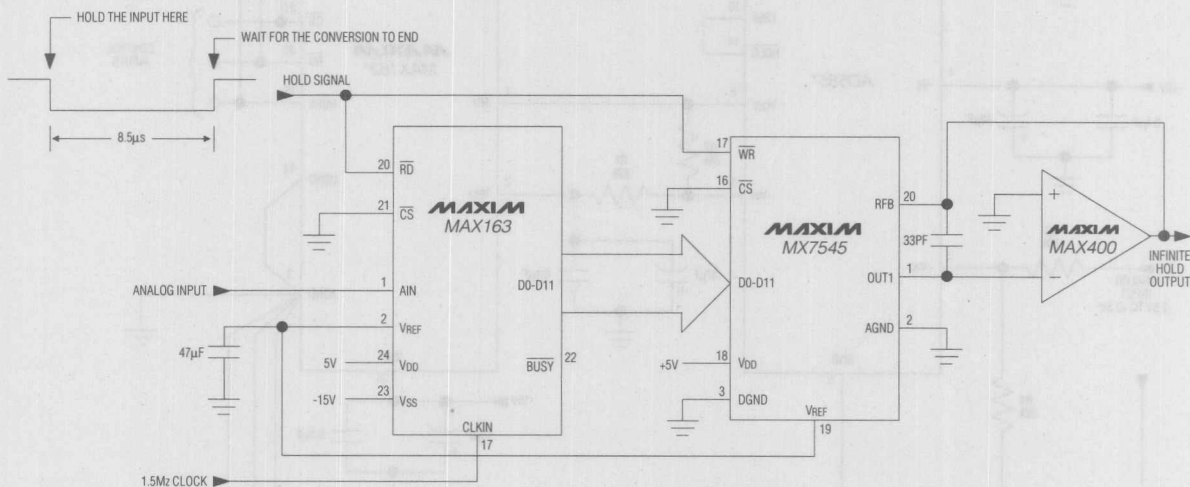


Figure 3-18. Infinite-Hold Sample-and-Hold

The analog input to a successive approximation ADC must be stable to within 1/2LSB during the conversion for specified 12 bit accuracy. This limits the input signal bandwidth to less than 6Hz for sinusoidal inputs. For higher bandwidth signals, a sample-and-hold should be used.

The $\overline{\text{BUSY}}$ output from the MAX162 provides the TRACK/HOLD signal to the sample-and-hold amplifier. However, since the ADC's DAC switches at approximately the same time the $\overline{\text{BUSY}}$ signal goes low, transients at the sample-and-hold output caused by DAC switching may result in code dependent errors due to sample-and-hold aperture delay. A NAND gate ensures that the sample-and-hold switches to hold mode BEFORE and disturbances. The width of the $\overline{\text{RD}}$ pulse must be wider than the $\overline{\text{RD}}$ to $\overline{\text{BUSY}}$ delay in the MAX162. If this is not possible, use a flip flop which is set by the falling edge of $\overline{\text{RD}}$ and reset by the rising edge of $\overline{\text{BUSY}}$.

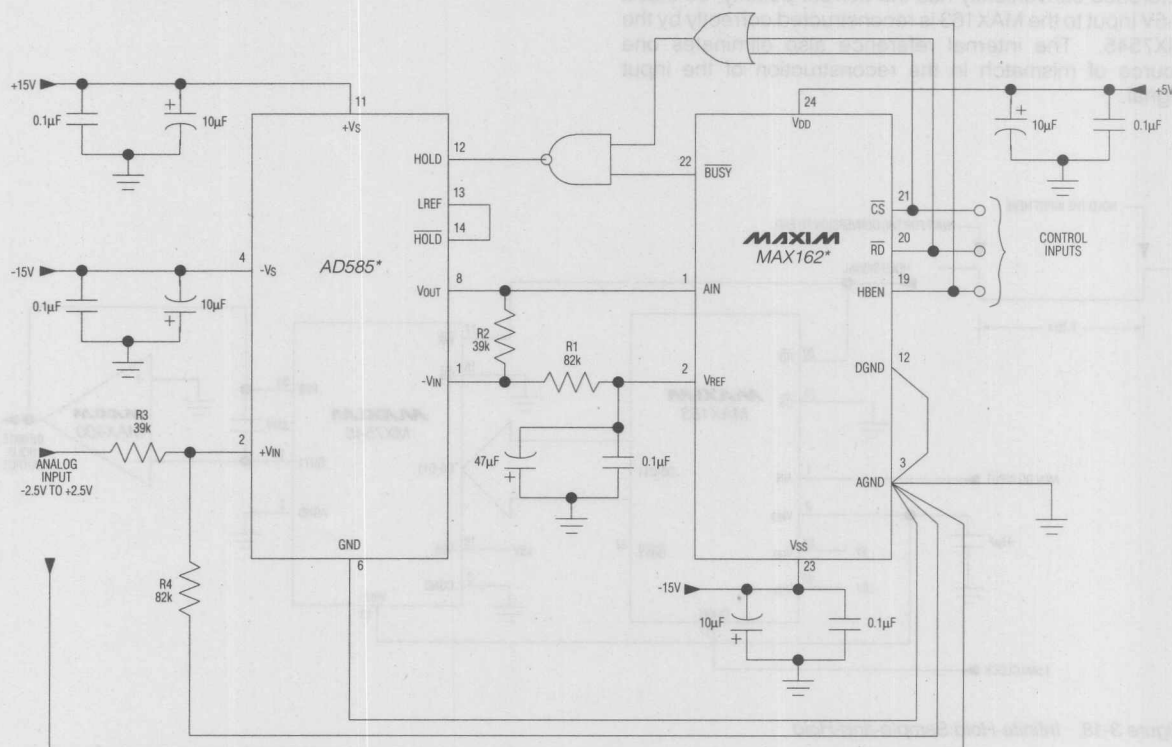
For synchronous $\overline{\text{RD}}$ and CLKIN as described above, the hold settling time allowed for the sample-and-hold is 500ns, 600ns and 1.5 μ s for the MAX162, MX7572XX05 and MX7572XX12 respectively.

For minimum sampling rate, the MAX162 data must be read within the time allowed for the sample-and-hold to acquire a new input voltage.

Figure 3-19 shows an AD585 sample-and-hold to MAX162 interface. The $\overline{\text{RD}}$ input and $\overline{\text{BUSY}}$ output put the AD585 in hold mode when a conversion is in progress. In this example the analog input range is $\pm 2.5\text{V}$ but other voltage ranges can also be configured.

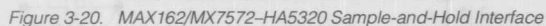
The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock allowing for a 3 μ s sample-and-hold acquisition time.

Although its circuit works quite well for the 1MHz clock rate, at the 2.5MHz clock rate a faster sample-and-hold amplifier such as the HA5320 is recommended.



* ADDITIONAL PINS OMITTED FOR CLARITY

Figure 3-19. MAX162-MX585 Sample-and-Hold Interfaces



Single Chip A/D With Track-and-Hold

The MAX167 is shown here in its "basic" application configuration because it offers nearly equivalent performance to the previous two A/D-plus-track/hold circuits, and does so with just one IC. It is also pin-compatible with the MAX162, MAX172, and AD7572. Complete conversion time, including track/hold settling, is $8.33\mu\text{s}$ with a 1.5MHz clock. Input signals beyond 59kHz can be digitized in real time, and due to the wide track/hold bandwidth, up to 6MHz periodic signals can be measured by undersampling. The MAX167 is trimmed for a $\pm 2.5\text{V}$ input range. The MAX163 and MAX167 accept 0-to-5V and $\pm 5\text{V}$ signals respectively.

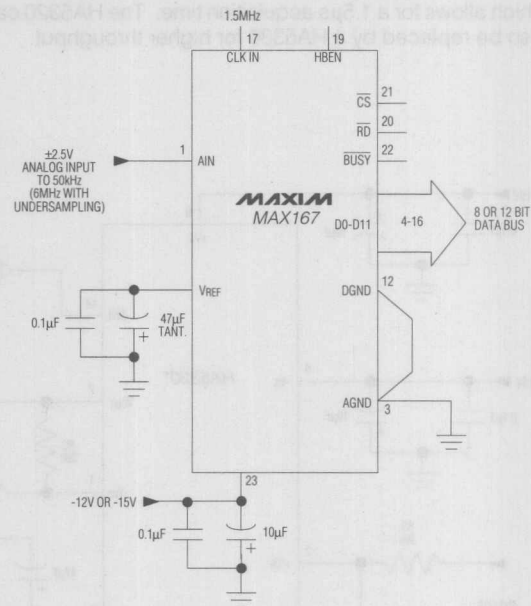


Figure 3-21.

Single +5V 12-bit A/D Operation

Because the MAX162/172 and MAX163/164/167 use only 135mW of power, they can easily be powered from a single +5V supply with the help of this low power DC-DC conversion circuit. A MAX636 generates a -12V (or a -15V) supply for the converter's V- input. A potential problem when using switching power supply circuitry with high speed A/Ds is increased noise but as the accompanying plot shows, the A/Ds' conversion noise is still quite low with this circuit.

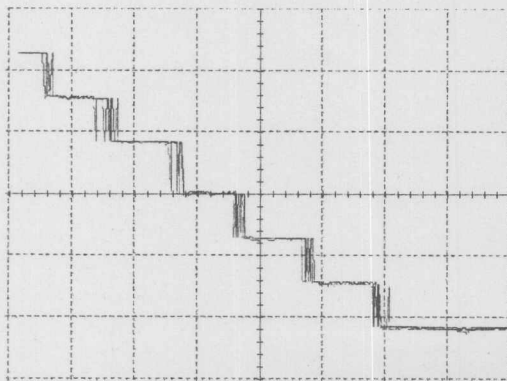
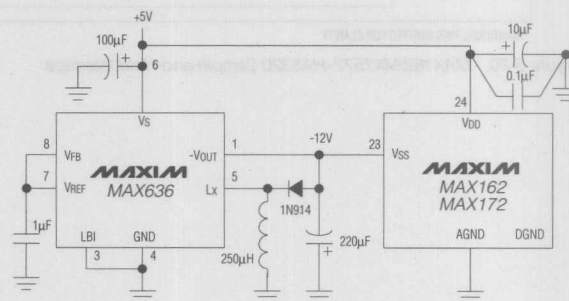


Figure 3-22.



ONLY POWER CONNECTIONS SHOWN FOR CLARITY

Figure 3-23.

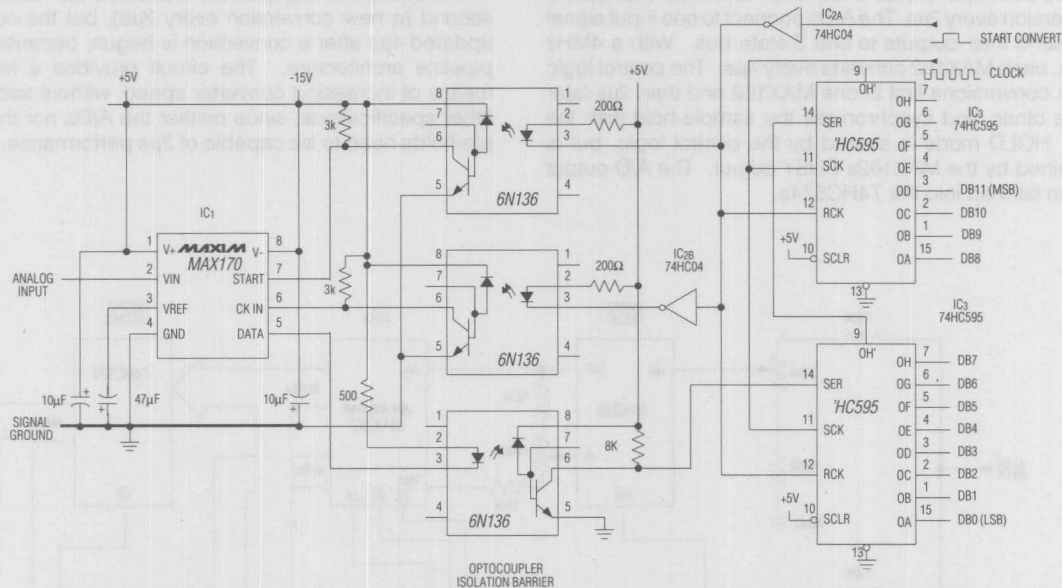


Figure 3-24. Serial data transmission from the A/D converter (IC1) simplifies this isolated conversion system by reducing the number of optocouplers required.

Conventional methods for transmitting analog signals across a voltage-isolation barrier involve isolation amplifiers based on optical, magnetic, or capacitive-coupling techniques. Maintaining DC performance and low noise, however, makes these amplifiers expensive. A less costly alternative, useful when the data is required in digital form, is to convert the signal on the isolated (or "cable") side of the barrier with an A/D converter, and then to pass the digital data across the barrier using optocouplers. The use of a serial-output converter simplifies this approach by reducing the required number of isolated lines to three (Fig. 3-24).

Start Convert and Clock inputs from the system (or "logic") side of the isolation barrier control the 12-bit, low-power A/D converter (IC1). Separate 6N136 optocouplers convey these two signals across the isolation barrier. A third 6N136 transmits the converter serial-output signal back to the system side, where shift registers IC3 and IC4 convert the bit stream to a 12-bit parallel output. IC2A and

IC2B assure adequate current drive to the optocouplers, which can withstand barrier voltages as high as 1500V.

Note that you must provide isolated power to the converter: 11mA max at 5V, and 8mA max at -15V. The converter produces 10,000 conversions per second when driven with a 140kHz clock. Faster optocouplers can increase this rate to the converter speed limit (over 100k conversions per second) by passing higher clock and data rates across the isolation barrier. Figure 3-25 illustrates system signal-timing relationships.

Noise pickup on the relatively slow optocoupler transitions can cause false triggering at the converter edge-sensitive Start input. To avoid this problem, set the rising edge of Start Convert to occur when the input ignores transitions, i.e., before the conversion ends. Making the Start Convert pulse at least two clock cycles long meets this condition. The falling edge of Start Convert triggers the next conversion, and also causes the results of the previous conversion to appear at the parallel data outputs.

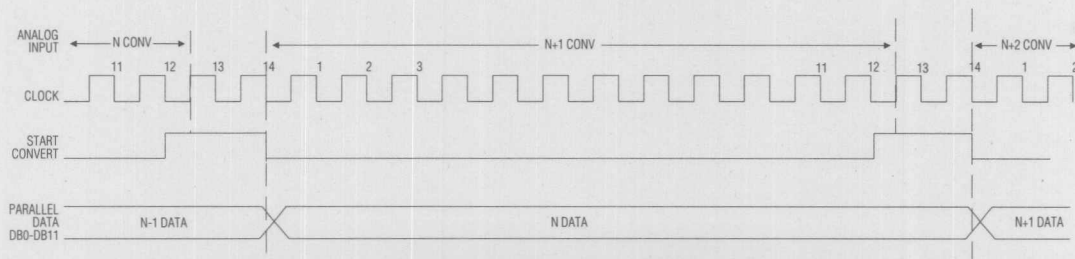


Figure 3-25. Start Convert pulses must repeat every 14 clock cycles to maintain data synchronization at the output. The falling edge of Start Convert should occur at the falling edge of Clock as shown. Clock can have any frequency up to 140kHz.

Two MAX162s create a low cost 12-bit A/D that does a conversion every $2\mu\text{s}$. The A/Ds connect to one input signal and send their outputs to one 3-state bus. With a 4MHz clock, each MAX162 converts every $4\mu\text{s}$. The control logic starts conversions first in one MAX162 and then $2\mu\text{s}$ later in the other, and synchronizes the sample-hold with the A/D. HOLD mode is started by the control logic, but is sustained by the MAX162s BUSY output. The A/D output is then latched into the 74HC574s.

The circuit's throughput rate is 500,000 conversions per second (a new conversion every $2\mu\text{s}$), but the output is updated $4\mu\text{s}$ after a conversion is begun, because of the pipeline architecture. The circuit provides a low cost means of increasing converter speed, without sacrificing other specifications, since neither the A/Ds nor the sample-holds need to be capable of $2\mu\text{s}$ performance.

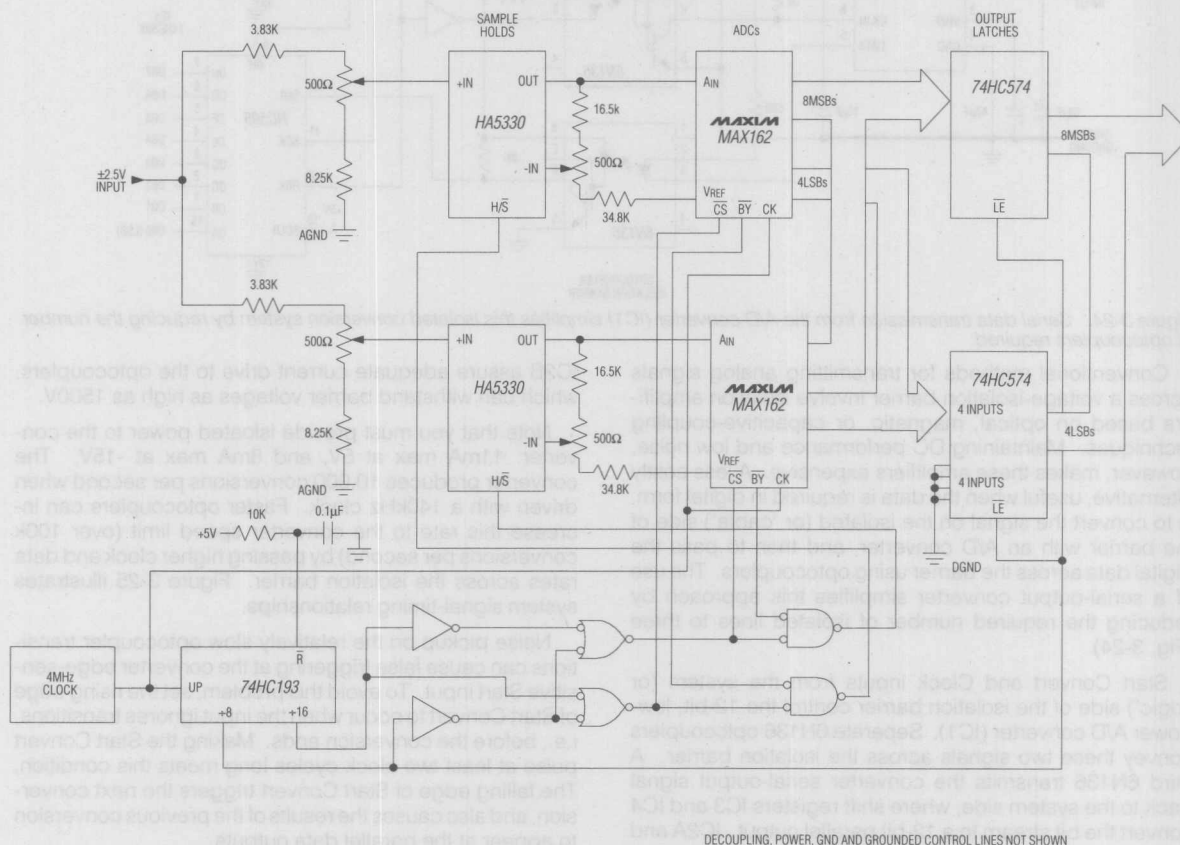


Figure 3-26.

The noise and linearity of high performance A/Ds can be tested without expensive measurement instruments using the circuit shown in Figure 3-27. A low amplitude triangle "dither" waveform is summed with a variable DC level and connected to the A/D. The 3LSBs of the converter output are summed together through 3 weighted resistors to make a 3-bit "DAC". The input signal and DAC output are connected to an X/Y oscilloscope so that a properly functioning A/D generates a staircase waveform. Eight bits of the A/Ds range can be viewed at one time and any part of the converter's input span can be checked by varying the DC level at the input. Output staircase waveforms from linear, noisy, and nonlinear 12-bit A/Ds are shown on the next page.

Since most of what is used in this test circuit is already included on a typical data acquisition board, a linearity "test point" could be added for in-circuit A/D testing by including a separate input resistor (at TP1) and the 3 output resistors (at TP2) on-board.

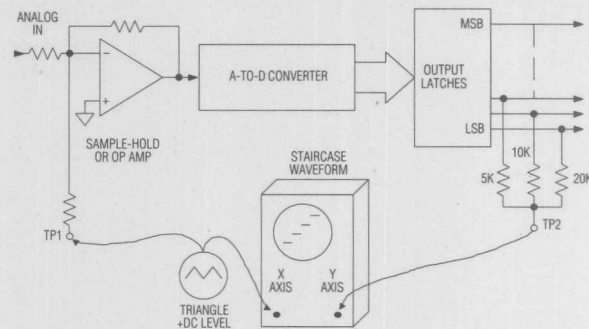


Figure 3-27.

Triangle Waveform Generator

This circuit generates a symmetrical 10mV p-p triangle waveform which is summed with a DC level and connected to the A/D analog input for noise/DNL testing. The DC LEVEL input offsets the triangle waveform over the input range of the A/D. The 10mV amplitude amounts to an 8LSB span for a 12 bit, 5V full-scale A/D.

The frequency of the sawtooth is critical, and depends on the speed of the converter to be tested. The frequency should be below the point at which the input moves 1/2LSB during a conversion (if there is no input sample-hold). Generally 10Hz to 1kHz is used. The $R1 \times C1$ product determines the sawtooth frequency. The oscilloscope "X" output is the same frequency, but is 3.3V p-p and is not affected by the DC LEVEL input.

Component values are not critical, and 5% values should work well. The ICL7641BCPD quad op-amp was used in our tests, but most other other quad op-amps will not alter the performance.

Take care to avoid noise on the sawtooth input to the ADC. Use short shielded cables, decouple the op-amp power supplies, and use single point grounding. Such precautions are needed because each 610 μ V of injected noise represents 1/2LSB.

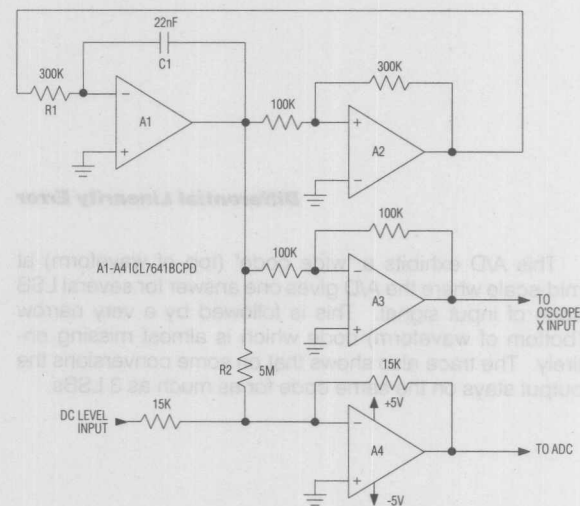
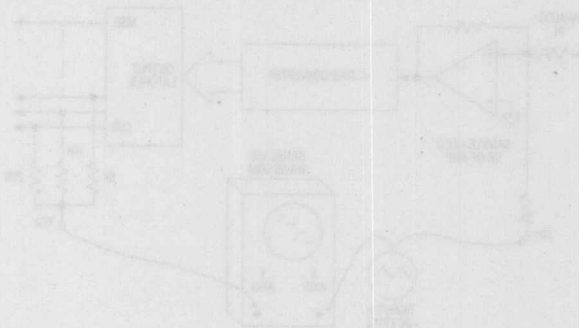


Figure 3-28.

Note the very small amount of overlap from one step to the next indicating less than 1/4 LSB of noise. Also, the uniform step size indicates low DNL error.



Noisy A/D

Here the step sizes are still relatively uniform but there is severe overlap and "bleeding" from one step to the next. With this particular converter, as many as 4 or 5 different conversion results are generated for one DC input.



Differential Linearity Error

This A/D exhibits a "wide code" (top of waveform) at mid-scale where the A/D gives one answer for several LSB span of input signal. This is followed by a very narrow (bottom of waveform) code which is almost missing entirely. The trace also shows that on some conversions the output stays on the same code for as much as 3 LSBs.

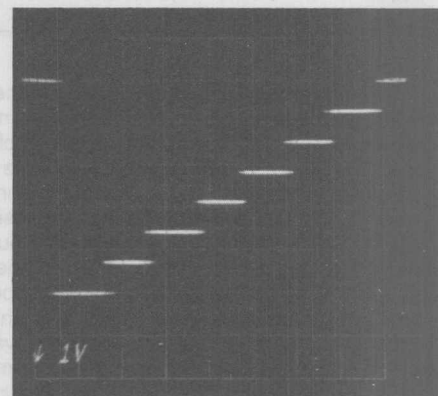


Figure 3-29.

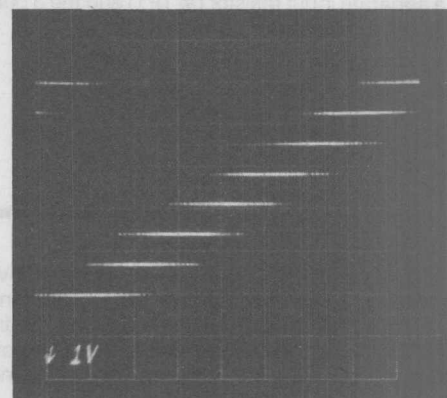


Figure 3-30.

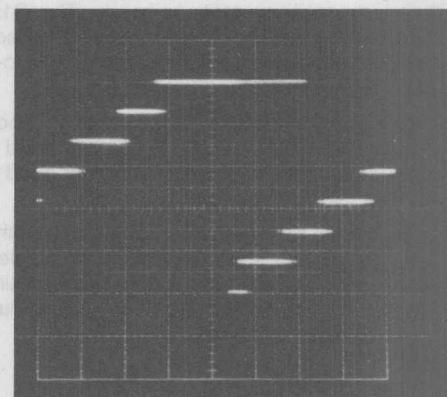


Figure 3-31.

With flash and successive approximation A/D converters, input transients can sometimes be observed on the analog input signal while the A/D is performing a conversion. Occasionally, attempts to filter this noise at the A/D input changes the converter calibration. Are these transients a problem, and if so, how should they be dealt with?

Many new CMOS A/D converter ICs use what is called "charge balanced" or sampling circuitry. This technique is becoming popular because it automatically corrects several internal A/D errors, like comparator offsets, which otherwise impair accuracy and linearity. The input transients referred to above are sometimes a side effect of charge balanced circuitry but, as explained below, they can usually be ignored without impairing A/D performance.

Part of the charge balanced input structure on many A/Ds is a small (1 to 35pF) capacitor inside the A/D that must be charged by the input signal. Depending on the type of A/D, the capacitor may get charged at each conversion (see Figure 3-32) or sometimes as often as every A/D clock cycle. The capacitor charging current flows into the A/D's analog input and sometimes generates a short voltage transient at the input terminal. The transient's size is related to the input signal's source impedance. The lower the source impedance, the lower the transient amplitude.

The A/D input is really the input of one or more comparators. Some time after the input capacitance starts charging, the comparator decision is digitally latched. This happens one time per conversion in flash converters, and several times per conversion in successive approximation converters. The length of this time depends on the speed of the A/D, and can vary from hundreds of nanoseconds to several microseconds. The key to remember is that A/D accuracy and noise is not affected as long as the input spikes settle before the comparator latches. In effect,

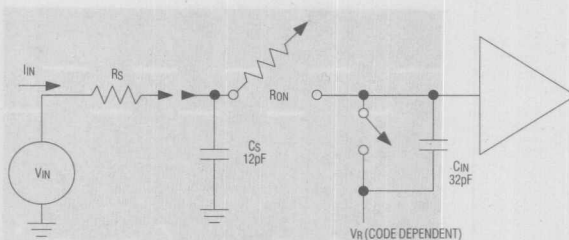


Figure 3-32. The input of some high speed CMOS A/Ds can be modeled as type of sample-and-hold. The 32pF input capacitance must be charged at each conversion. V_R is code dependent but is nominally 2.5V. The input current is: $I_{IN} = \text{Conv./sec} \times (V_{IN} - V_R) \times C_{IN}$

charge balanced A/Ds are designed not to "look" at the input while the transient occurs.

If the input spike settles before the A/D "looks", then no filtering is needed. Leaving this transient unattended may not seem like the best low noise "solution", but there are really no adverse effects from doing just that, as long as the spike settles in time. In fact, filtering with a capacitor at the A/D input can actually create a gain error by integrating the spike energy from a time when the A/D is not "looking" at the input signal to a time when it is.

If the spikes do not settle in time, then the source impedance of the signal is probably too high. Many A/Ds have a maximum specification for this, ranging from a few ohms to several kilohms. The only solution to this impedance problem is to add a low output impedance buffer or op-amp between the signal source and the A/D. Once this is done, there are no longer restrictions on filtering, because it can be done at the buffer input rather than the A/D input terminal.

MAX150 INPUT

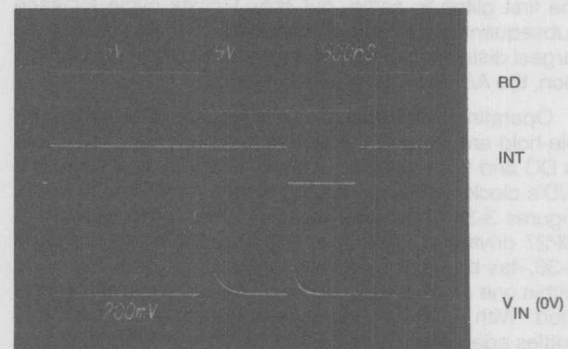


Figure 3-33.

The photo of Figure 3-33 shows the READ input, INTERRUPT output, and the analog input of a MAX150 running at 250,000 conversion/sec. The input signal is OV through a 1k Ω source resistance. R_S is larger than recommended to highlight the input transient. Again, no conversion error is generated by these spikes as long as they are allowed to settle before the internal comparators are latched (approx. 600ns in the READ interface mode). The second transient in the photo occurs after the conversion is finished (when INT goes low) and has no effect.

Figure 3-34 illustrates the disturbance at the input pin of a MAX162 12-bit A/D that is clocked at 1MHz. The input is being driven by an OP27 amplifier. The amplitude of the pulse disturbances at the input generally decrease as the conversion takes place. This is because the reference DAC's output transitions become smaller as the A/D zeroes in on the answer.

If the driving device (op-amp or sample-hold) does not accommodate the load changes presented by the A/D, the voltage at the analog input terminal deviates from the desired value for a short time. These "glitches" are synchronous with the ADC clock and may be 10mV or more in amplitude. Even though 10mV is well above 1LSB in amplitude, the pulses do not degrade the A/D's performance **IF** they settle before the comparator's output is sampled at the next falling clock edge.

If the open loop output impedance of the driving amplifier is too high (enabling the glitches to be generated), or if its settling time is too long (enabling the glitches to persist for more than a clock cycle), some errors may be generated even with slow moving input signals. It is interesting to note in the photos that the MAX162 allows 1 1/2 clock cycles for the first glitch to settle, but only 1 clock cycle for each subsequent pulse. This is intentional. Since potentially the largest disturbance occurs at the first bit test in the conversion, the A/D allows more settling time.

Operating symptoms of an inadequate op-amp or sample-hold are missing codes when the analog input signal is DC and free of noise. A good test is to slow down the A/D's clock, giving the driving device more time to settle. Figures 3-35 and 3-36 show this test in practice with an OP27 driving the A/D input. With a 4MHz clock (Figure 3-36, 4 μ s between conversions) the OP27 does not settle within one clock period, and conversion errors are generated. With a 2MHz clock however (Figure 3-25), the OP27 settles adequately and 1LSB performance is achieved.

If the desired conversion rate is below the A/D's limit, amplifiers with less than optimum output specifications may be used. The A/D clock of course has to be slowed. The approximate speed at which various op-amps can perform adequately with the MAX162 is listed on the following page. There is some performance variation between devices made by different manufacturers of the same device type.

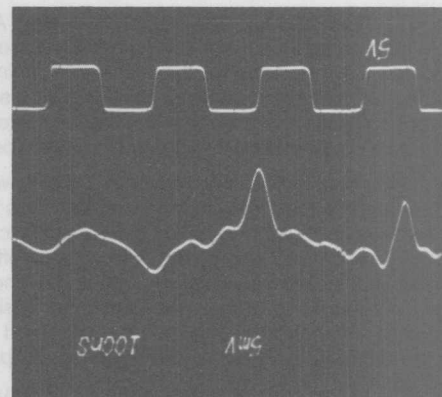


Figure 3-34. 1MHz Clock

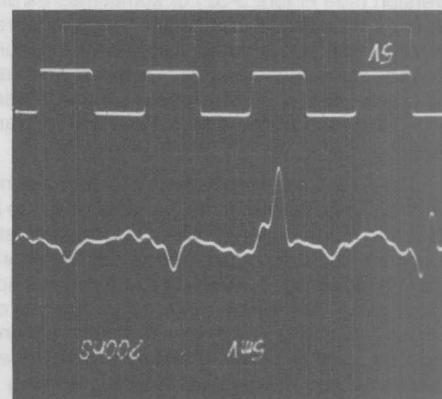


Figure 3-35. 2MHz Clock

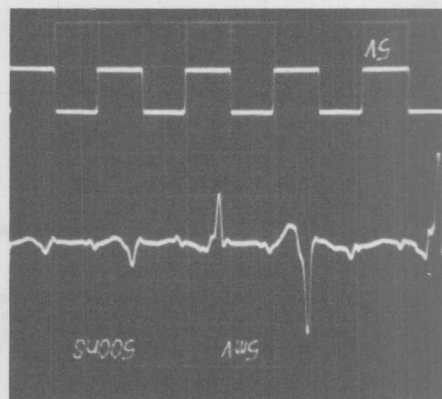


Figure 3-36. 4MHz Clock

Things to watch for when picking an op-amp to drive the MAX162 or MX7572 are:

- Thermal tails on output settling are a frequent characteristic of "high slew rate" op-amps with undefined settling specs.
- Amps with 0.01% settling specs usually do substantially better than those with only 0.1% numbers.
- Input offset voltage and offset drift.
- High frequency PSRR – This affects settling time but unfortunately is not specified by many manufacturers.
- Some general purpose amplifiers will work reasonably well as input buffers at reduced A/D clock rates:

CA3140, OP27 –	1/2LSB DNL at 0.6MHz 1LSB DNL at 0.7MHz
LT1055, LF411 –	1/2LSB DNL at 0.6MHz 1LSB DNL at 0.7MHz 2LSB DNL at 2MHz

The amplifier-A/D combination should be checked with a faster A/D clock than the design requires.

A SAR A/D input is typically driven by an op-amp or sample-and-hold, however, care must be taken with high speed A/D like the MAX162, because it's tempting to assume that

high frequency input signals can be converted accurately with no sample-and-hold. A 12-bit converter with a 5V full scale range resolves input changes of nearly 1mV, and signals as slow as 1kHz change by this amount in well under the 3.25ms conversion time of the MAX162. In fact for full-scale signals above only 11Hz, some sort of hold function has to be added if the conversion is to be accurate to 12 bits.

The acceptance criteria for sample-holds suitable for use with the MAX162 are:

- Aperture time fast enough to capture the highest input frequency – 30ns will preserve the MAX162's performance,
- Acquisition time of about 500ns,
- Hold step error (switching glitch) of less than 1/2LSB (i.e., less than 600 μ V),
- Hold droop less than 1/2LSB in the cycle time of the ADC (often about 4 μ s),
- Input offset voltage <600 μ V over temperature range.

If an off-the-shelf sample-and-hold is required, the HA5330 is a good match for the performance of the MAX162. Its offset error, acquisition characteristics, and output stability are all sufficient to avoid degrading the accuracy of the MAX162.

This is the analog portion of a digital multimeter. The precision attenuator resistors on the left side are connected to a set of kelin-sensed analog switches which are controlled by the microprocessor through bits in the MAX133 control registers. The analog switches are controlled by the microprocessor to select 400mV, 4V, 40V, 400V, and 4000V ranges. The external AC-DC converter can be bypassed for DC measurements or inserted into the signal

path for AC measurements, again under the control of the microprocessor. Similarly, the selection of the current input and control of the active filter are also controlled by the microprocessor.

The MAX133/134 does all of the critical timing related to the actual A/D conversion, but higher level control and setup functions are controlled by the microprocessor via the MAX133 control register bits.

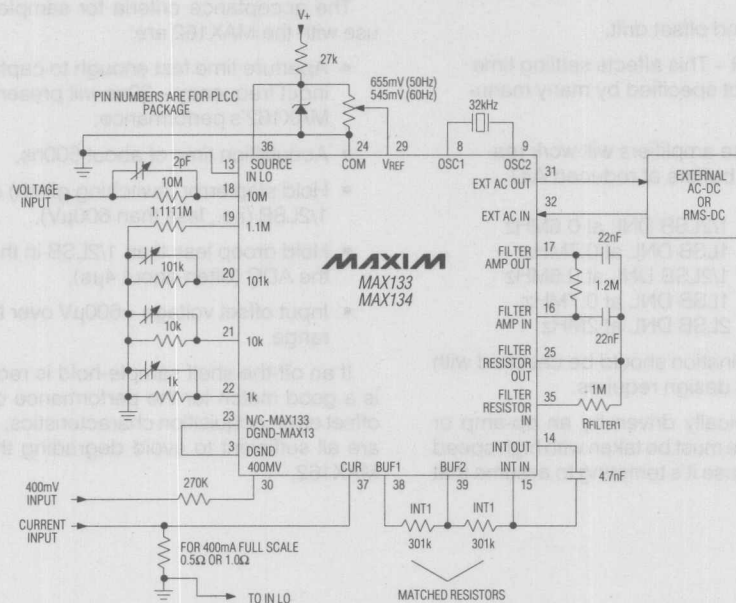


Figure 3-37.

+5V Powered DVM with $\pm 3.5V$ Input Range

The MAX138, MAX139, MAX140 allow DVM functions to be easily included in single +5V powered boards. Either analog input may operate above or below ground, facilitating direct measurements of ground referenced signals (or current shunts) in single supply systems. These parts accomplish this by generating their own V- supply with an internal charge pump. Up to 1mA may be drawn from the chip's V- output (approximately -4.8V) to power other circuitry. Here, a +5V logic supply is used to power a MAX139 and LED display. The same approach can be used with LCDs and low current LEDs by using the MAX138 and MAX140, respectively.

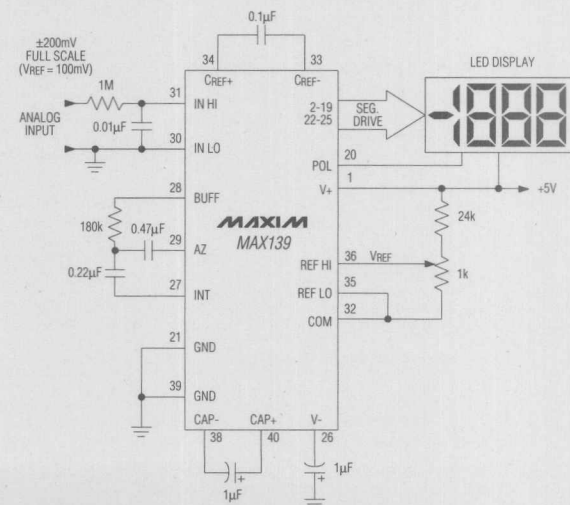


Figure 3-38.

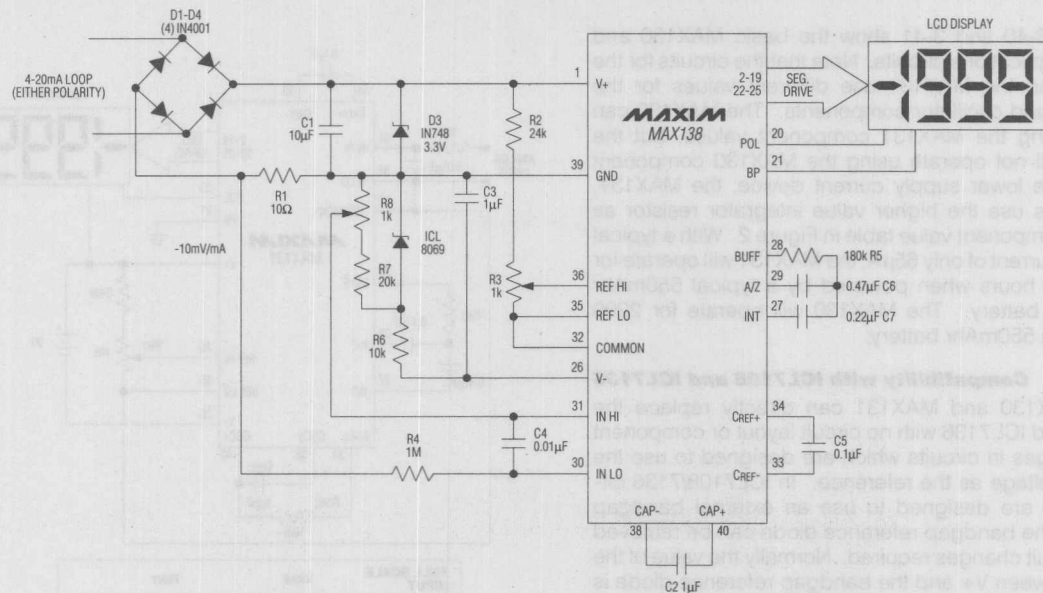


Figure 3-39.

The unique features of the MAX138 allow it to be used in low voltage applications that were previously not feasible for display driving A/Ds. In this example, a 0-100.0% digital indicator (LCD) measures, and is powered from, an industrial 4-20mA analog current loop. The circuit consumes only 4.5V when inserted in the line. A full-wave bridge at the input allows either input polarity to be measured, but if the input polarity is known, the full-wave bridge can be omitted, reducing the circuit's operating voltage.

A voltage proportional to the loop current is developed across a 10Ω sense resistor, R1. A 3.3V zener clamps the MAX138's supply as the current through the loop changes. IN HI (pin 31) is offset negatively and trimmed by R8 so that the display reads "000.0%" with 4mA loop current. R6 is set for an indicator of "100.0%", with a 20mA loop current. R8 and R6 can also be adjusted so the display reads directly in milliamps.

Figures 3-40 and 3-41 show the basic MAX130 and MAX131 applications circuits. Note that the circuits for the MAX130 and the MAX131 use different values for the integration and oscillator components. The MAX130 can operate using the MAX131 component values, but the MAX131 will not operate using the MAX130 component values. The lower supply current device, the MAX131, must always use the higher value integrator resistor as shown in component value table in Figure 2. With a typical operating current of only 65 μ A, the MAX131 will operate for about 8500 hours when powered by a typical 550mAh alkaline 9V battery. The MAX130 will operate for 2200 hours with a 550mAh battery.

Compatibility with ICL7106 and ICL7136

The MAX130 and MAX131 can directly replace the ICL7106 and ICL7136 with no circuit layout or component value changes in circuits which are designed to use the Common voltage as the reference. In ICL7106/7136 circuits which are designed to use an external bandgap reference, the bandgap reference diode can be removed with no circuit changes required. Normally the value of the resistor between V+ and the bandgap reference diode is the only component value that must be changed to allow the removal of an external bandgap reference diode.

Single 5V Supply Operation

Figure 3 shows typical components for +5V single supply MAX130/131 operation with a 200mV full scale range. Since the common voltage is 3.05V below V_+ , it is less than 2V above ground. This means that the integrator swing must be reduced by increasing the value of the integrator

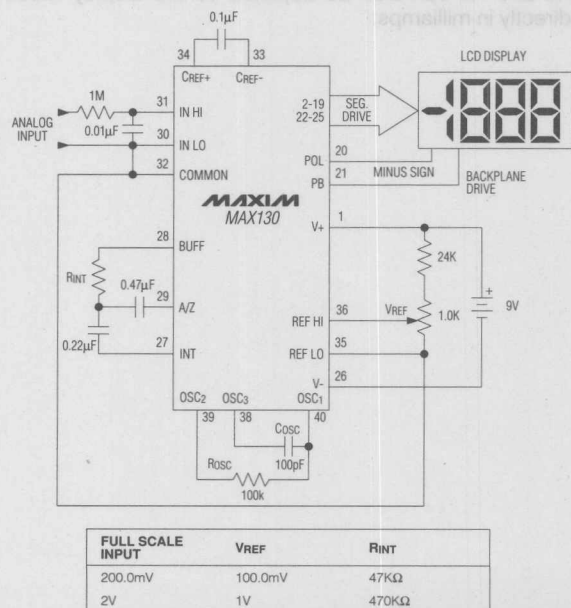


Figure 3-40. Maxim MAX130 Typical Operating Circuit, 3 Conversions per Second

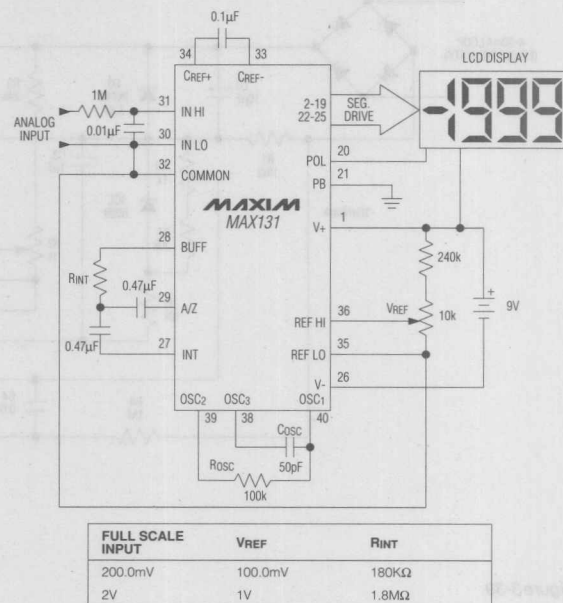


Figure 3-41. Maxim MAX131 Typical Operating Circuit, 3 Conversions per Second

capacitor. The value shown will result in about 1V to 1.5V integrator swing.

The voltage at the buffer input must stay in the common mode voltage range of $(V_- + 1.5V)$ to $(V_+ - 1.5V)$. With the maximum common mode voltage of 3.15 and a full scale negative input of -200mV, this limit is met with a 4.85V or greater supply.

With a +2V full scale, the input buffer will exceed its negative common mode voltage range when a -2V input is applied with less than 6.7V supply voltage.

Operation on $\pm 5V$ Supplies

The MAX130/131 can easily be used with $\pm 5\text{V}$ supplies. Connect V_+ to $+5\text{V}$, V_- to -5V . If the voltages to be measured are referred to ground, then connect IN LO to ground. In most cases, REF HI and REF LO should be connected to a resistive divider string between V_+ and Common, as shown in the standard application circuits of Figures 3-40 and 3-41. If Common is not used to generate the reference it can either be left floating or can be connected to ground. If the MAX130/131 LCD oscillator is driven by 5V logic, or if the MAX130/131 LCD outputs drive 5V logic, then connect the Test pin to ground. If the MAX130/131 open circuit Test voltage is above ground, then connecting Test pin to ground will set the internal digital ground to approximately ground. If, however, the open circuit Test voltage is negative, then the internal digital ground voltage will remain negative, additional V_+ supply current will be drawn, and the LCD segments will continue to swing below ground. The OSC1 pin, however, will respond to a voltage swing of 0V to 5V in either case.

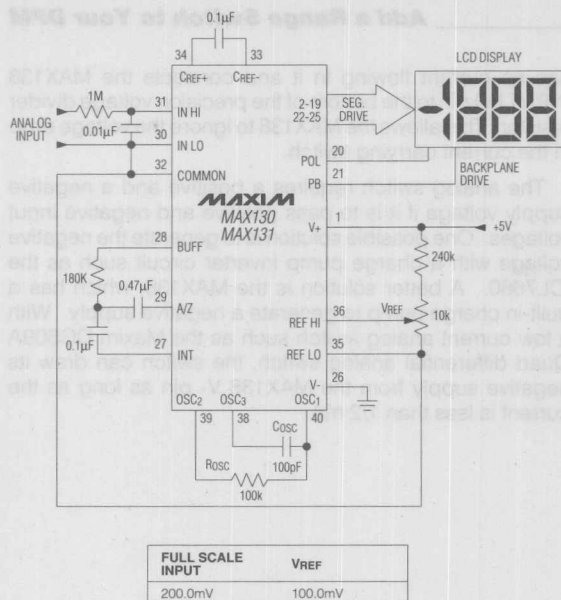


Figure 3-42. Single Supply +5V Operation

Low Battery Detector Circuits

Since the voltage between Common and V+ is between 2.95V and 3.15V until the voltage between V+ and V- falls to less than 4V, a simple low battery detector can be made using a transistor voltage detector as shown in Figure 4. When Q2 is off the Low Battery segment is driven in phase with the backplane and is off. When Q1 and Q2 turn on, the Low Battery segment is held approximately midway between the Test voltage and V+, and the Low Battery LCD segment becomes visible. Q1 and Q2 turn on when the voltage at the base of Q1 is one base-emitter voltage more positive than Common voltage. With the 4.7MΩ/4.7MΩ divider shown, this occurs when the battery voltage is

approximately 6V. Decrease the value of R1 to lower the battery detection voltage.

A similar circuit using only one transistor can be made using the Test pin as the reference voltage rather than the Common. Since the Test pin voltage may range from 4V to 6V, the low battery detection voltage when using the Test pin as a reference is not as accurate as shown here, where the Common voltage is the reference.

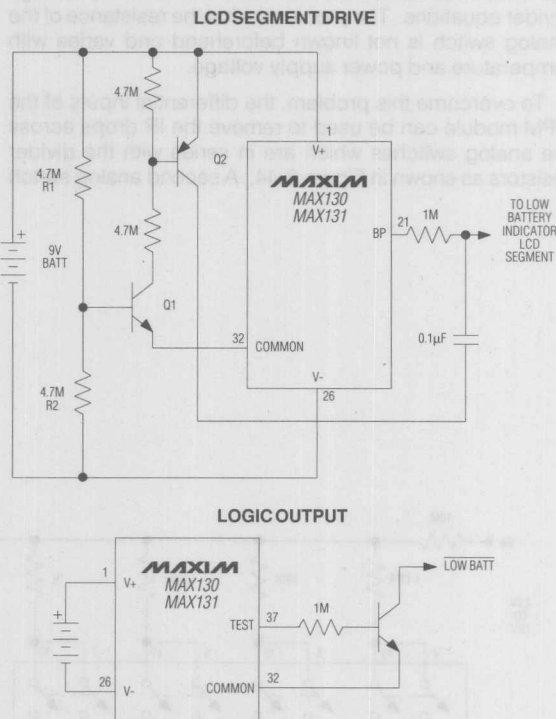


Figure 3-43. Low Battery Detectors

There are many single chip Digital Panel Meter chips and modules available today at low cost. However, these meters are limited to a single input voltage range and cannot select different voltage ranges. This feature can be added by connecting a switched voltage divider to the input of the DPM. If solid state analog switches are used, the switch resistance must be considered in the voltage divider equations. The problem is that the resistance of the analog switch is not known beforehand and varies with temperature and power supply voltage.

To overcome this problem, the differential inputs of the DPM module can be used to remove the IR drops across the analog switches which are in series with the divider resistors as shown in Figure 3-44. A second analog switch

has no current flowing in it and connects the MAX138 INPUT LO pin to the bottom of the precision voltage divider resistor. This allows the MAX138 to ignore the voltage drop in the current carrying switch.

The analog switch requires a positive and a negative supply voltage if it is to pass positive and negative input voltages. One possible solution is to generate the negative voltage with a charge pump inverter circuit such as the ICL7660. A better solution is the MAX138, which has a built-in charge pump to generate a negative supply. With a low current analog switch such as the Maxim DG509A Quad differential analog switch, the switch can draw its negative supply from the MAX138 V- pin as long as the current is less than 1/2 mA.

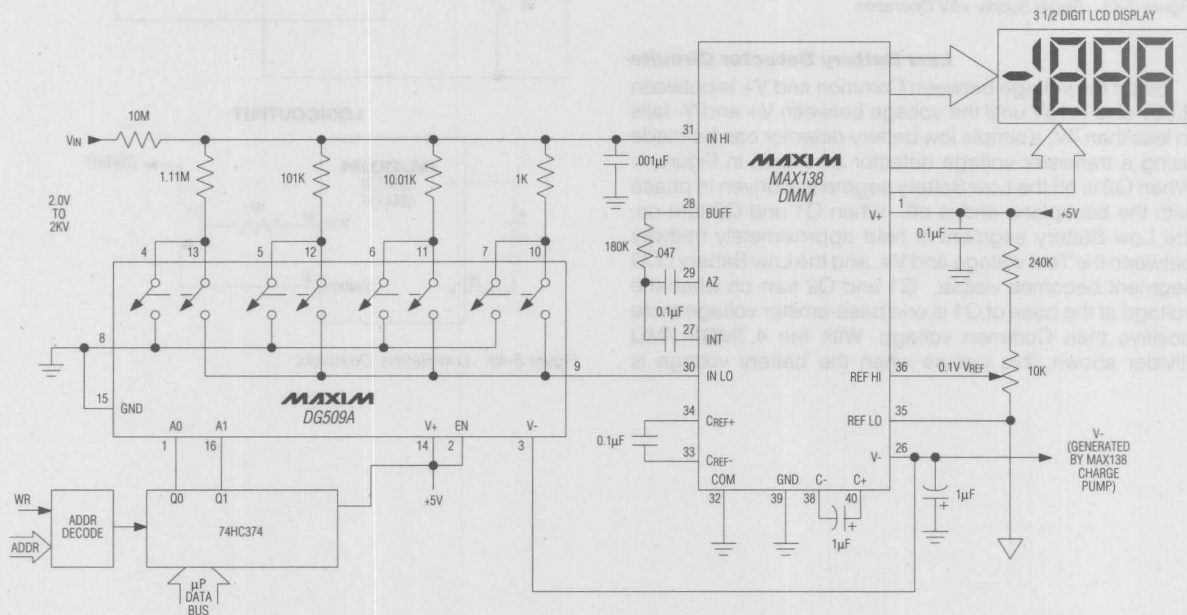


Figure 3-44.

You can build a simple, compact digital thermometer using a single-chip thermometer amplifier such as the MX594. This device includes cold-junction compensation and provides a laser-trimmed, 10mV/°C output for type J or K thermocouples. The MX594 can operate with a single positive supply, but to measure negative temperatures it must have a split or bipolar supply – not a welcome requirement in portable applications.

By combining the MX594 with a DVM chip that generates its own negative supply (IC2) you can implement a portable, 2-chip digital thermometer that operates on a single battery. IC2 includes a charge-pump circuit that inverts the applied positive-supply voltage and produces a negative voltage of the same magnitude. This supply voltage (available on pin 26) provides as much as 0.5mA to external loads such as the MX594.

These devices work well together because the MX594's negative-supply terminal draws only 300µA maximum. With a liquid-crystal display and a 6V supply, the resulting thermometer can measure and display temperatures from -350 to 400°C. With a 3V lithium battery, the range is -50 to 100°C.

Accuracy depends primarily on IC1, whose output voltage is rated $\pm 1^\circ\text{C}$ for A-suffix versions and $\pm 3^\circ\text{C}$ for C-suffix versions. You can improve these specs by adding a trimpot adjustment as described in the data sheet. A suitable external reference (in place of the 100ppm (max) bandgap reference in IC2) provides more stable readings, as does the use of low-tempco resistors for R2 and R3.

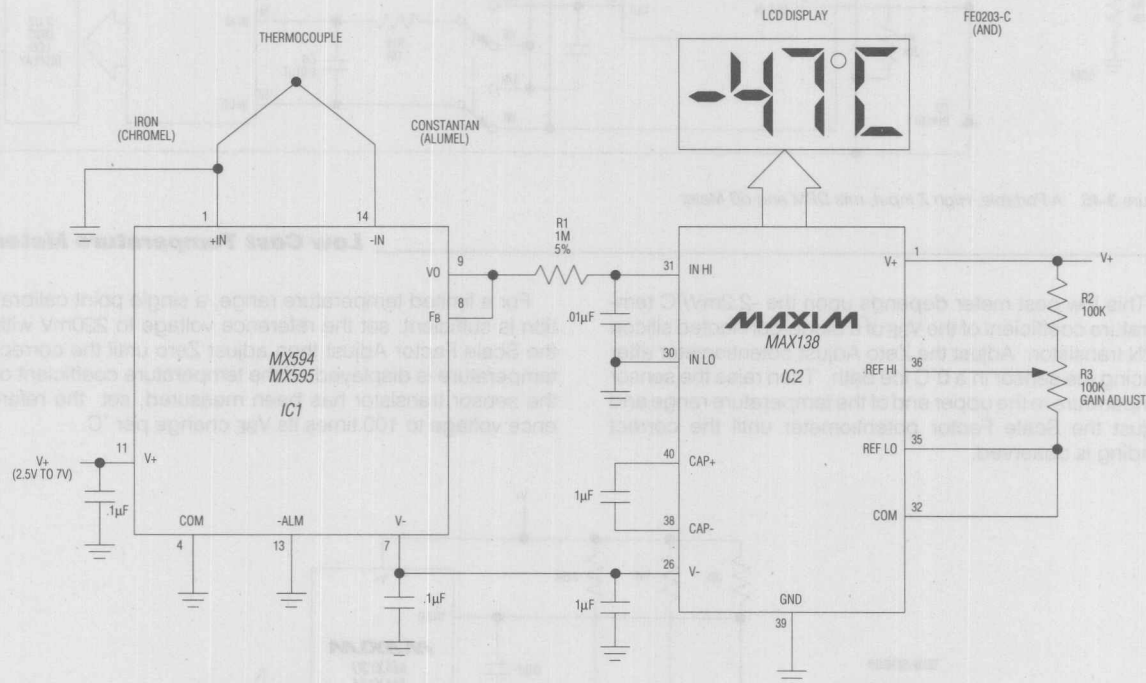


Figure 3-45. This portable digital thermometer measures positive and negative temperatures, yet requires only a positive supply voltage (V+). The V- supply generated within IC2, accessible at its filter-capacitor terminal (pin 26), provides the negative voltage needed by IC1.

A low cost true RMS reading AC digital voltmeter using just two integrated circuits plus supporting circuitry and LCD display is shown. The MAX130 is a 3 1/2 digit integrating A/D converter with precision bandgap reference. The input attenuator is AC coupled to pin 6 of the MX636 buffer amplifier. The output from the MX636 is connected

to the MAX130 to give a direct reading to the LCD display. The circuit shown will exhibit some noise with MAX131 in the dB mode due to the MAX131 internal charge pump oscillator. Add a lowpass filter to the dB $\rightarrow$ IN LOW signal path.

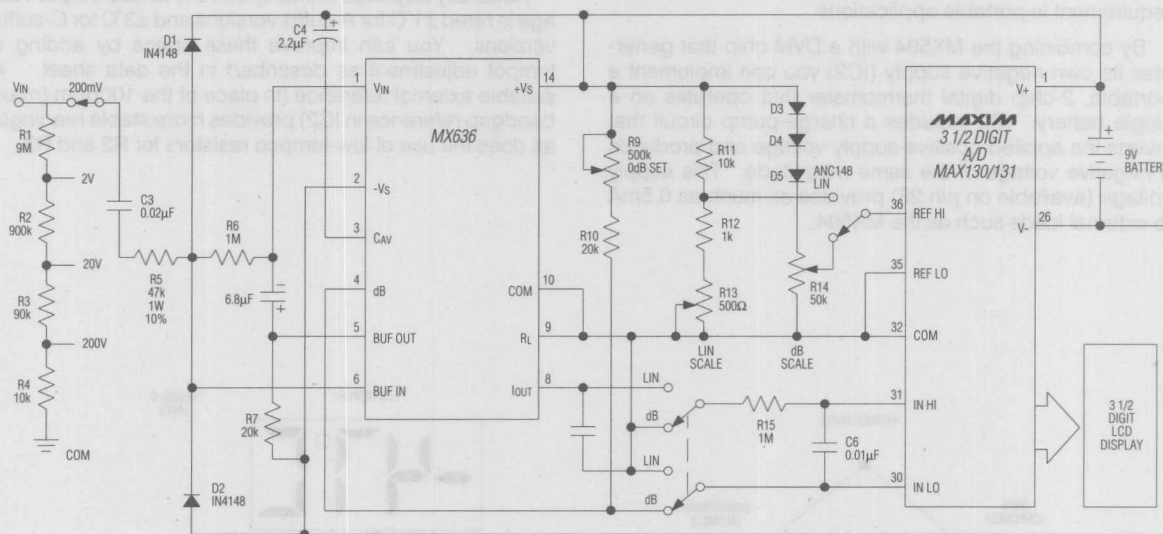


Figure 3-46. A Portable, High Z Input, rms DPM and dB Meter

Low Cost Temperature Meter

This low cost meter depends upon the $-2.2\text{mV}/^\circ\text{C}$ temperature coefficient of the V_{BE} of a diode-connected silicon NPN transistor. Adjust the Zero Adjust potentiometer after placing the sensor in a 0°C ice bath. Then raise the sensor temperature to the upper end of the temperature range and adjust the Scale Factor potentiometer until the correct reading is observed.

For a limited temperature range, a single point calibration is sufficient: set the reference voltage to 220mV with the Scale Factor Adjust then adjust Zero until the correct temperature is displayed. If the temperature coefficient of the sensor transistor has been measured, set the reference voltage to 100 times its V_{BE} change per $^\circ\text{C}$.

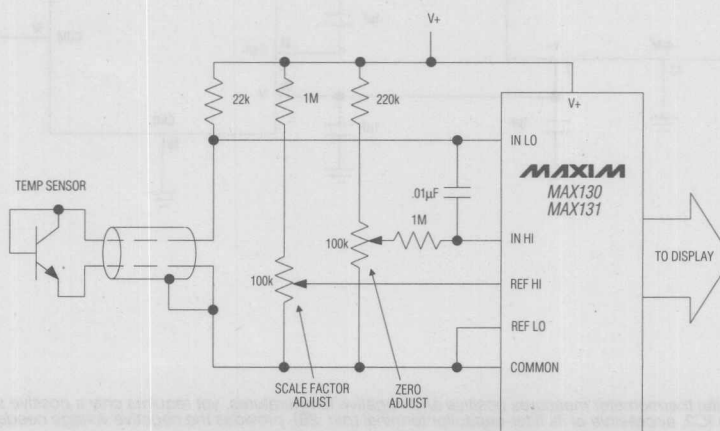


Figure 3-47.

The common platinum resistance sensor (also called PT100, RTD, or PRT) is a repeatable, stable, and reliable sensor. It is, however, nonlinear. This circuit compensates for the nonlinearity by adding a correction signal to the reference voltage via the op-amp A.

Op-amp B provides a zero offset correction by making the voltage at Input Low equal to the voltage at Input High when the RTD resistance is equal to that of R_0 . Since the MAX136 is used in the ratiometric mode, no voltage reference is needed.

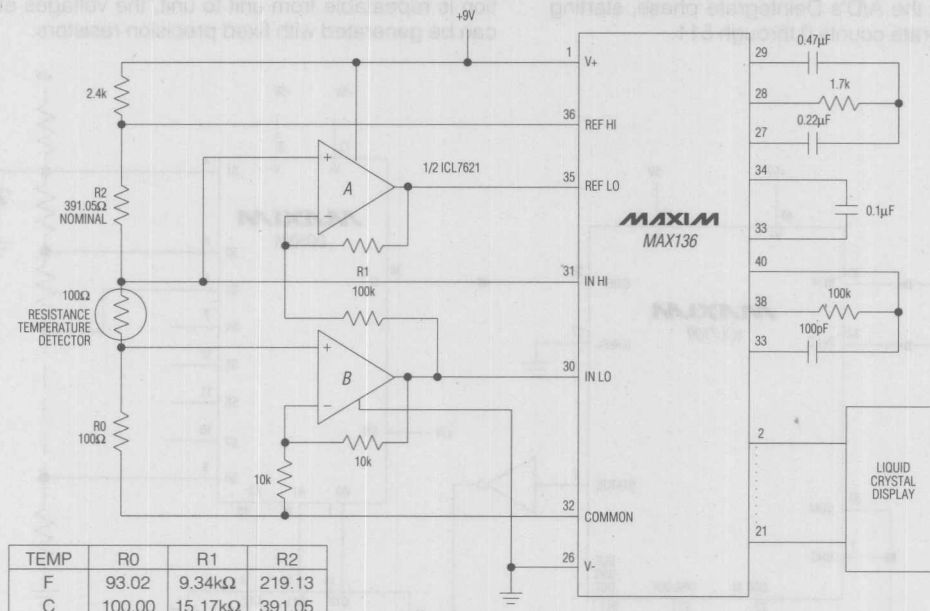


Figure 3-48.

Operating DVM A/Ds without Reference Capacitor

Usually, the reference capacitor is used as a floating voltage source to provide either a positive or negative reference during the de-integrate phase, depending on the polarity of the input signal. If the input signal always has the same polarity, the reference capacitor can be eliminated by feeding the reference voltage directly into the CREF pins.

For inputs that are always positive, connect CREF+ to Common and CREF- to a negative reference voltage. If the input voltage is always negative, connect CREF- to Common and apply a positive reference to CREF+.

This circuit can also be used to perform a "1/X" function, where the displayed reading is inversely proportional to the voltage being measured. For 1/X readings, connect the voltage to be measured to the CREF- (+ or -) terminal, and feed a fixed negative reference voltage into IN HI. Typical applications include RPM meters and conductance meters.

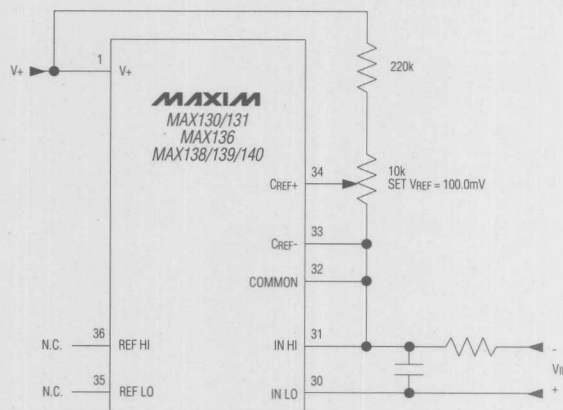


Figure 3-49.

voltage, and therefore the slope, of straight line segment is selected by an 8-channel multiplexer, DG508A. The ICL7109 Clock and Busy signals drive a CD4040 counter such that a different reference voltage is selected for each 512 counts during the A/D's Deintegrate phase, starting with S1 for Deintegrate counts 0 through 511.

responding to approximately 512 counts. Then adjust the voltage at S2 for the correct reading with an input corresponding to approximately 1024 counts. Continue this procedure for S3 through S8. If the sensor's output function is repeatable from unit to unit, the voltages at S1-S8 can be generated with fixed precision resistors.

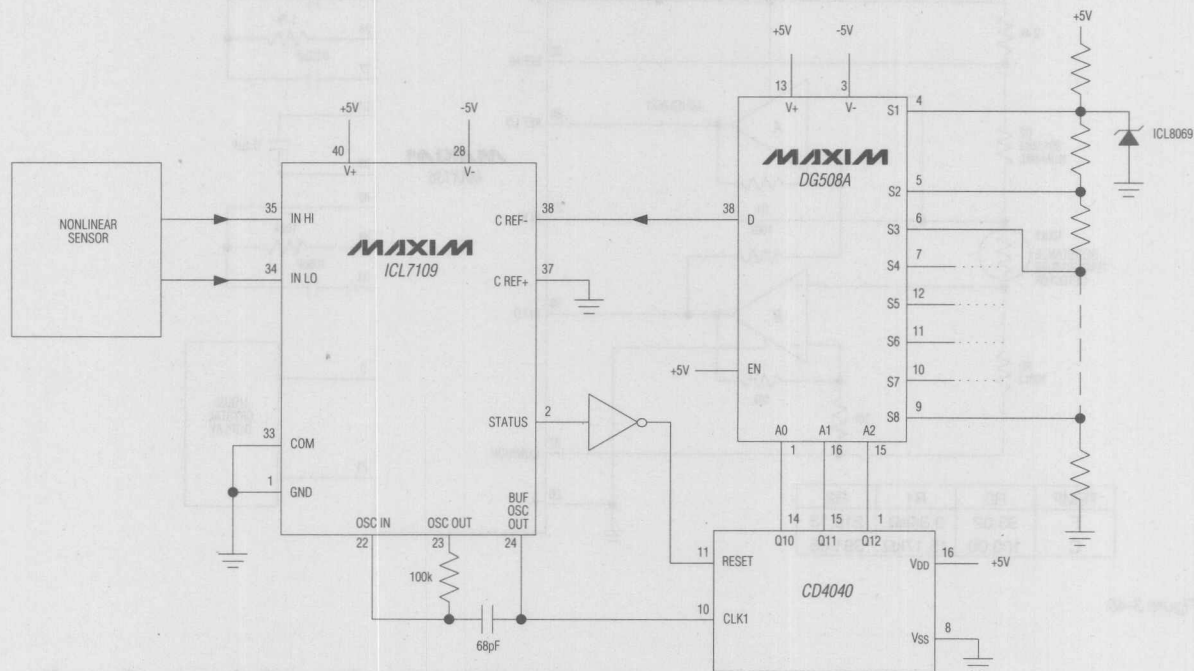


Figure 3-50.

This circuit displays the logarithmic ratio of two input voltages, V_1 and V_2 . The ratio of R_1 and R_2 should be precisely 1 to 9. Calibrate the circuit by adjusting R_P for a reading of 10.00 when $V_1 = 10 V_2$.

Typical applications include audio level measurements, densitometry, and colorimetry. The resistor R_P in parallel with the integrate capacitor makes the voltage waveforms on the capacitor exponential rather than the linear ramps of the normal configuration.

Unlike normal, linear operation, the accuracy of this circuit depends on both the ratio and the absolute value of the external components.

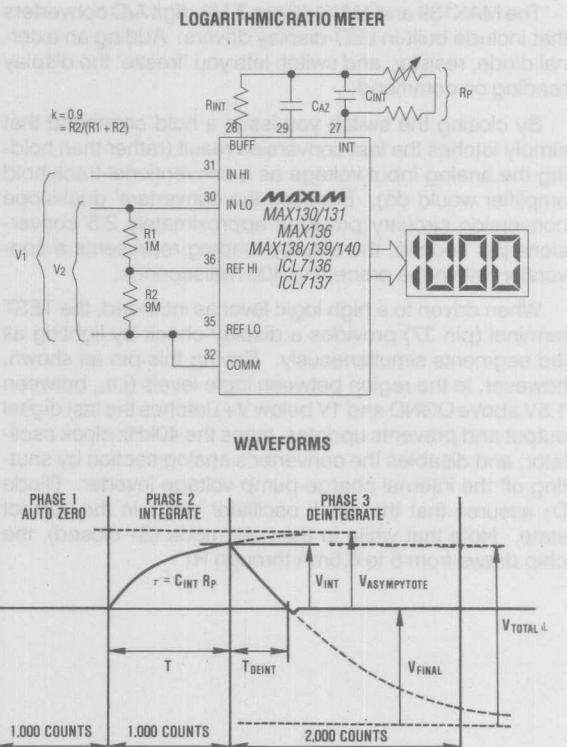


Figure 3-51.

Extending A/D Common Mode Range

The input range of most integrating A/Ds is limited to approximately 1.5V below V_+ and 1.5V above V_- . However, since the A/D's input impedance is high, differential signals with common mode voltages outside the chip's power supplies can be easily measured. This is done by connecting a resistive voltage divider to each input pin.

In this example, the current from a +24V supply, flowing to a grounded load, is measured by sensing the differential signal on a current sense resistor at the 24V source. This signal is divided by identical voltage dividers at the A/D HI and LO inputs. The resulting measurement may be scaled by adjusting either the sense resistor or the A/D reference to correct for losses from voltage divider attenuation.

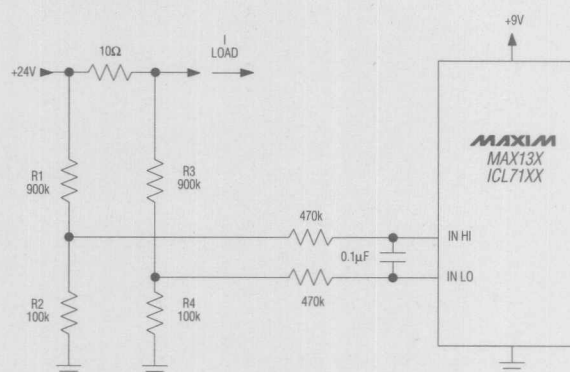


Figure 3-52.

The MAX139 and MAX140 are 3 1/2-digit A/D converters that include built-in LED-display drivers. Adding an external diode, resistor, and switch lets you "freeze" the display reading on command.

By closing the switch you issue a hold command that simply latches the last conversion result (rather than holding the analog input voltage as a conventional track/hold amplifier would do). Because the converters' dual-slope conversion circuitry provides approximately 2.5 conversions per second, the display reading represents a conversion within the preceding 400 milliseconds.

When driven to a high logic level as intended, the TEST terminal (pin 37) provides a display check by lighting all led segments simultaneously. Driving this pin as shown, however, to the region between logic levels (i.e., between 1.5V above DGND and 1V below V+) latches the last digital output and prevents updates, stops the 40kHz clock oscillator, and disables the converter's analog section by shutting off the internal charge-pump voltage inverter. Diode D₁ assures that the clock oscillator stops in the correct state. Note that while in the hold mode (S₁ closed), the chip draws from 5 to 6.5mA through R₁.

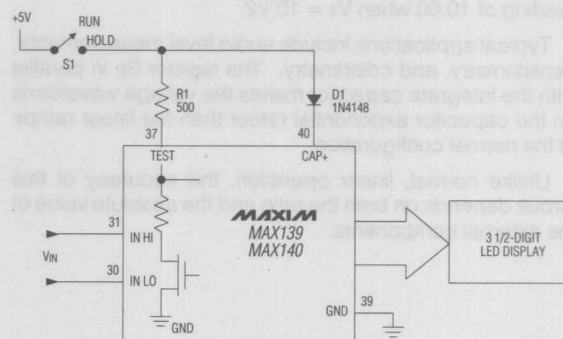


Figure 3-53.

This simple digital thermometer is turned on by opening the refrigerator door via a photoresistor. When the refrigerator door is closed, the circuit draws less than $1\mu\text{A}$.

The photoresistor (R5) is high resistance when the refrigerator light is off. This turns off the n channel MOSFET (Q1) and shuts down the rest of the circuit. When the photoresistor is illuminated, Q1 turns on and supplies the ground voltage to the rest of the circuit.

The MX590 PTAT (Proportional To Absolute Temperature) current generator forces $1\mu\text{A}/\text{degree Kelvin}$ into the MAX480 summing junction. Resistor R4 offsets the current for the more conventional Centigrade thermometers. R3 then converts the current into a voltage ($10\text{mV}/^\circ\text{C}$) and

feeds this into the IN HI terminal of the MAX138. The MAX138 is a 3 1/2-digit dual slope converter which takes this voltage and drives the display with 0.1°C resolution. The total power dissipation is approximately 400µA when the circuit is active and <1µA when disabled.

To calibrate the system, insert the MX590 into an ice bath and adjust R4 resistor to read zero. IF R3 is a 0.1% resistor, then adjusting the REF HI to REF LO voltage (RRF1) to 1.000V will calibrate the scale factor. Otherwise boiling water can provide the scale adjustment.

Also note that the battery generally will last twice as long in the refrigerator due to the cold.

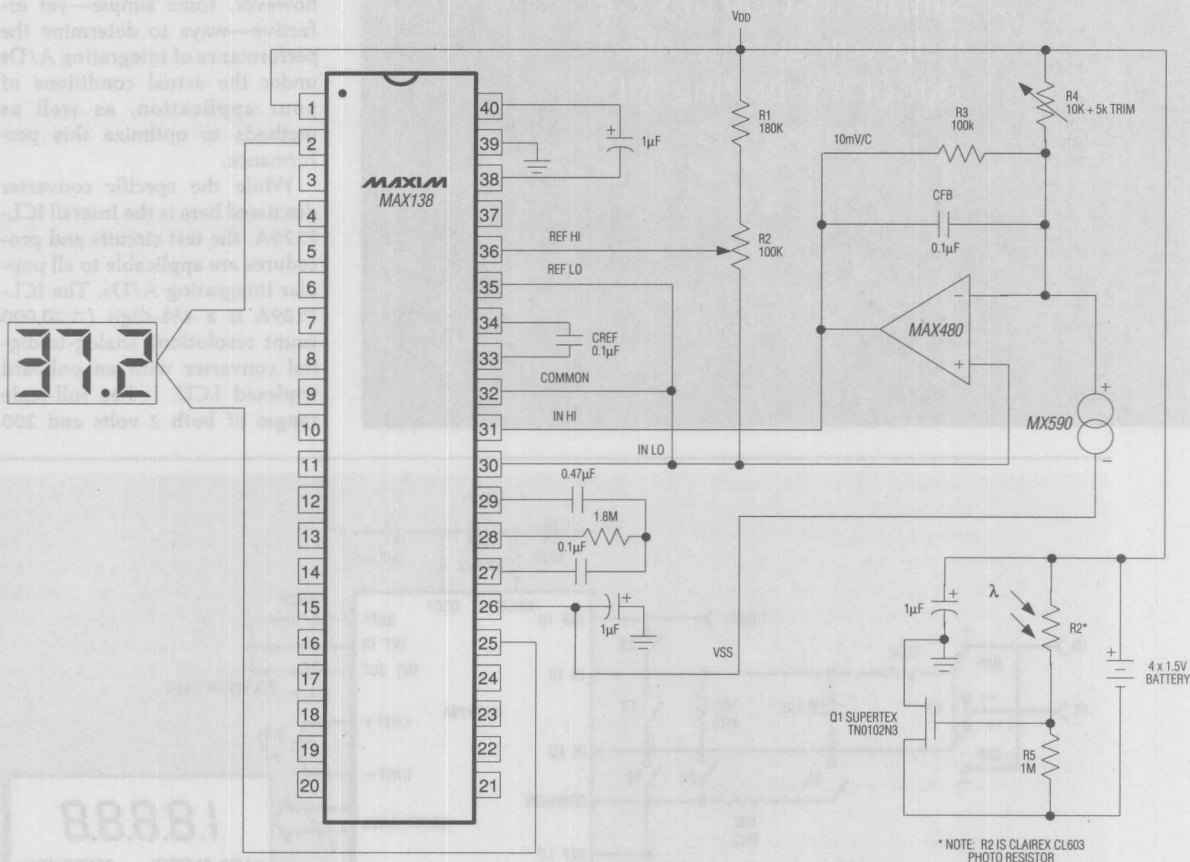


Figure 3-54.

How will your A/D really perform?

Simple test circuits can help you get the most out of integrating A/D converters.

Charlie Allen
Maxim Integrated Products
Sunnyvale, California

Integrating analog-to-digital (A/D) converters offer high accuracy, nearly ideal differential nonlinearity, high power supply rejection, and low cost. As such, they're often used in digital multimeters, temperature meters, process control gear, and data acquisition systems.

In many of these diverse applications, integrating A/Ds are often used under conditions other than those for which the converter is specified. There are, however, some simple—yet effective—ways to determine the performance of integrating A/Ds under the actual conditions of your application, as well as methods to optimize this performance.

While the specific converter discussed here is the Intersil ICL7129A, the test circuits and procedures are applicable to all popular integrating A/Ds. The ICL7129A is a $4\frac{1}{2}$ -digit ($\pm 20,000$ count resolution) analog-to-digital converter with an onboard triplexed LCD. It has full-scale ranges of both 2 volts and 200

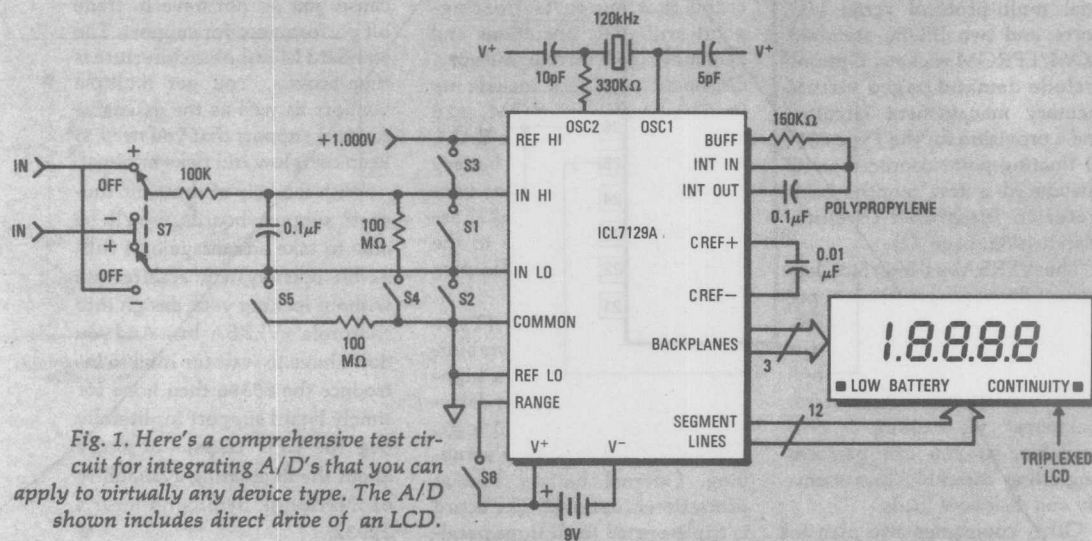


Fig. 1. Here's a comprehensive test circuit for integrating A/D's that you can apply to virtually any device type. The A/D shown includes direct drive of an LCD.

millivolts, with 10 microvolt resolution on the low scale.

The Test Circuit

The test circuit shown in Figure 1 allows you to directly test many of the key specifications of the ICL7129A and other integrating A/Ds. Details are shown in the accompanying table.

A high-resolution input-voltage source is required to measure A/D noise. This voltage source must also have good short term stability but need not be a high-accuracy source. A $6\frac{1}{2}$ -digit voltage calibrator, if available, makes an ideal source. However, you can also make an acceptable input voltage source by summing a coarsely-adjusted voltage source with an attenuated "dither" voltage (Figure 2).

Similar to the "dither DAC" arrangement, often used to test successive-approximation A/Ds, the dither voltage is attenuated by a factor of 100 and added to the coarse voltage source before being applied to the A/D.

Measure the dither voltage

with a $4\frac{1}{2}$ -digit multimeter before attenuation. This provides an effective resolution of $6\frac{1}{2}$ -digits referred to the input of the A/D under test. (The resolution of the input voltage source is $\frac{1}{100}$ count of the $4\frac{1}{2}$ -digit A/D under test.)

Noise Management

Noise is one of the most difficult parameters to measure quantitatively. Yet, it is often the primary factor in selecting an A/D converter IC. Most integrating A/Ds specify a "peak-to-peak noise not exceeded 95 percent of the time." This value is 3.3 times the RMS noise, assuming Gaussian distribution.

The observed effect of noise is jitter, or flicker of the least significant digit (Figure 3). If the peak-to-peak noise is greater than one count, the A/D will display three different results for some input voltages.

When the noise is exactly one count, the display will jump back and forth between two adjacent digits. At $\frac{1}{2}$ count, the display

will jump back and forth between adjacent digits when the input voltage is within $\pm\frac{1}{4}$ of one count of the transition point between displayed counts, and will show a single reading when the noise is not close to a transition point.

To measure noise using the transition detection method, first adjust the input voltage until the A/D displays one reading almost all of the time, with only an occasional display of the next higher reading. The higher reading should occur approximately once every 20 conversions. Record the input voltage.

Next, adjust the input voltage upward until the higher reading is displayed for almost every conversion, with only an occasional display of the lower reading. Record this second input voltage. The peak-to-peak noise is simply the difference between these two readings.

Use Care

The primary problem with this method is that it tends to be sub-

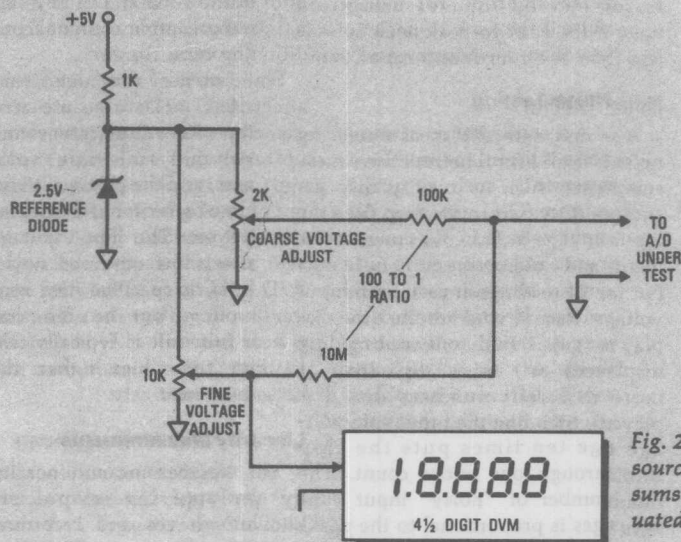


Fig. 2. This high-resolution voltage source for testing A/D converters sums a coarse voltage with an attenuated "dither" source.

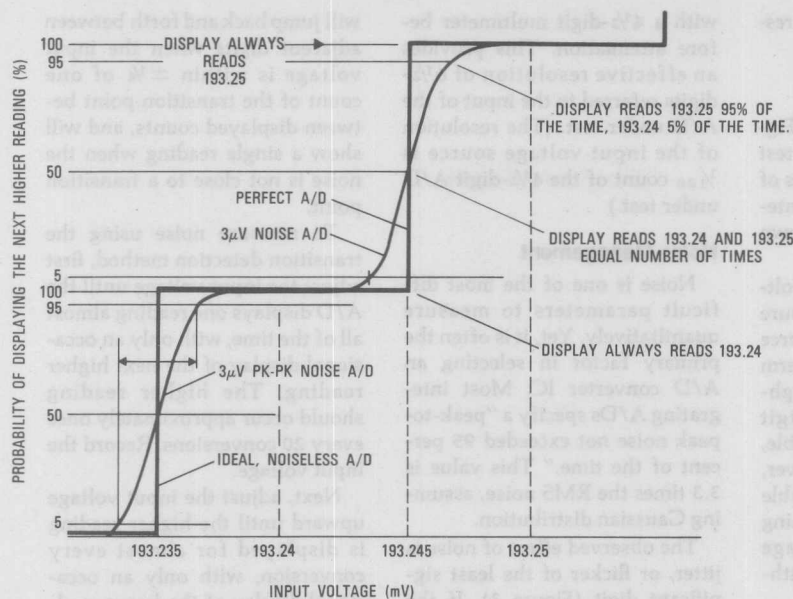


Fig. 3. Noise causes A/Ds to have a transition region, where more than one reading is displayed for a fixed input voltage. Noise is defined as the width of this transition band, measured from the 5 to 95 percent points.

jective; it is very difficult to determine the exact voltage where the adjacent reading is displayed once per 20 conversions. A second problem is that measurements take several minutes per device. Nonetheless, this method gives accurate results when carefully performed. It's the preferred method for measuring noise if the peak-to-peak noise is less than one-fourth of a count.

Noise Testing

A second method of measuring noise is useful for repetitive measurements, such as quality assurance (QA) screening. Step the input voltage in $\frac{1}{10}$ count increments and observe the A/D output for 20 readings at each input voltage. Record whether the display is "quiet" (only one reading displayed) or "noisy" (two or more different numbers displayed). Stepping the input voltage ten times puts the chip through one entire count. The number of "noisy" input voltages is proportional to the peak-to-peak noise.

For example, if the A/D has noise of $\frac{1}{2}$ count, the display will typically have jitter on five of the ten input voltages applied. If the peak-to-peak noise of the A/D is only 0.2 count, the display will typically be stable for eight of the ten input voltages and alternate between adjacent counts with two of the input voltages.

Due to the random nature of noise, repeated measurements of the same device may result in different readings. The average result of several measurements will be the true noise of the device under test.

This method requires little judgement on the operator's part, and about 15 units per hour can be sample tested. Since the noise of an integrating A/D is relatively constant for all devices in a given lot, a sample size of five units is sufficient to characterize each lot.

In addition to evaluating the noise level of A/Ds from various manufacturers, these noise test methods let you determine the effect of circuit design changes, both in the A/D and in any signal preamplification or signal conditioning circuitry.

Some of the many items that affect A/D noise are auto-zero capacitor values, integrator swing voltages, full-scale input voltages, and the physical circuit layout of analog buffer and integrator sections. The input voltage also affects the observed noise. A/D noise is specified near zero input voltage, but the noise that is near full scale is typically two to three times higher than the noise near zero.

Linearity Measurements

You can measure nonlinearity by applying several precise, known voltages and recording the conversion results. The max-

imum deviation from a "best fit" straight line through the measured points is the sum of the nonlinearity error plus quantizing errors of up to one-half count. The quantizing error term can be eliminated by finding the transition points where two adjacent codes are each displayed 50 percent of the time.

For example, if the display is flickering back and forth between 0009 and 0010, with each reading being displayed about 50 percent of the time, the digital output code is considered to be 0009.5. Accurate nonlinearity measurement requires the use of either a $6\frac{1}{2}$ -digit voltage calibrator or a calibrated $6\frac{1}{2}$ -digit meter to measure the voltage applied to the A/D converter.

Zero Code Width Measurement

Integrating A/Ds with sign magnitude output format have two zeros: +0000 and -0000. To have a linear transfer func-

tion between input voltage and displayed readings, these two zero codes should each be one-half the width of normal codes (Figure 4). Using the standard circuits shown in data sheets, the delay of the A/D zero-crossing comparator is about half a clock cycle. This narrows the width of the zero codes to the desired half-count width. Keep in mind that operating the A/D at a different clock rate or with significantly different component values will affect the zero code width and thus should be evaluated.

You can determine the width of the plus and minus zero codes by applying a small voltage to the input and adjusting this voltage until equal numbers of zeros and ones are displayed.

A better way to test for zero offset is to find the transitions between +0009 and +0010. The zero offset is the difference in magnitude between the measured transition points. To de-

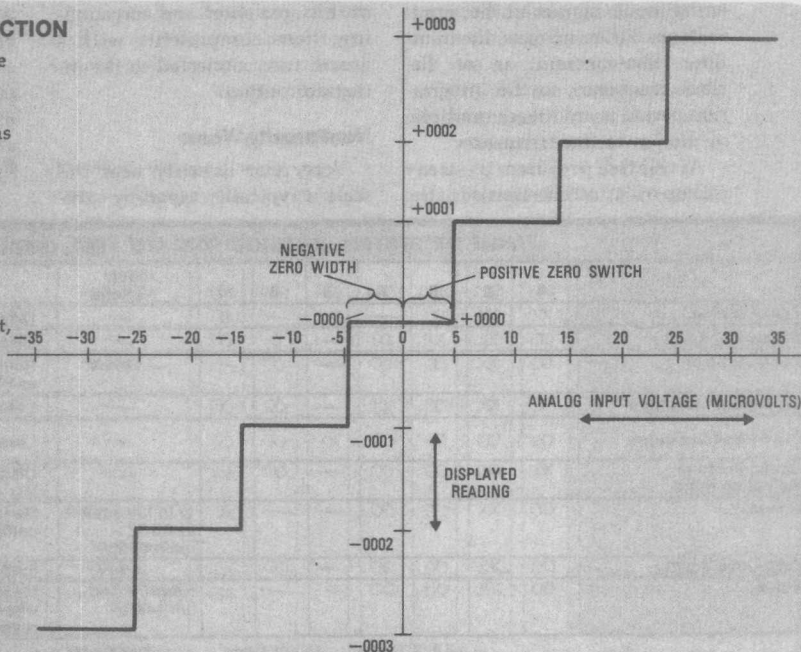
termine the zero code width, compare the measured transition points with the desired transition point.

For 200 millivolts full scale, the ideal transition point between 0009 and 0010 is 95 microvolts. Measuring a transition point five to twenty counts away from zero is the preferred method of measuring zero-offset and zero-width. The first few counts around zero may have additional nonlinearities caused by op-amp settling. This may happen when transients occur as a result of the A/D switching from the signal-integrate phase to the reference-deintegrate phase.

Placing a low-value resistor in series with the integrating capacitor can help you adjust the zero-code width of many analog-to-digital converters. The voltage across this resistor causes the input voltage to the comparator to cross earlier than the true zero-crossing. It thereby com-

THE A/D TRANSFER FUNCTION

This example shows the discrete steps in the A/D output. The transfer function of an ideal integrating A/D around zero has two zeros, +0000 and -0000, each of which is $\frac{1}{2}$ the width of the other count widths. The delay of the A/D zero crossing comparator shortens the zero code width to $\frac{1}{2}$ count, putting the zero-to-one code transition at the desired 5-microvolt point, rather than at 10-microvolts. Since the comparator delay is a fixed time period, it becomes a large fraction of the clock period as the clock frequency is increased in order to perform more conversions per second. At very high conversion rates, the zero code will disappear. Under standard data sheet conditions, this A/D is guaranteed to display +0000 or -0000 with a zero volt input.



pensates for the comparator delay.

There are several different causes of excessive noise. Look at the integrator output voltage during a conversion. A very low integrator voltage swing reduces the signal-to-noise ratio at the comparator input, increasing the A/D converter noise. The integrator output should swing to within one to two volts of the power supply voltage when you apply a full-scale input voltage.

Next, make sure that the auto-zero capacitor is at least twice the value of the integrator capacitor. This ensures that the noise of the auto-zero loop will be negligible compared to that of the buffer and integrator. (This precaution does not apply to the ICL7129A, which reduces overall system noise by digitally compensating for the A/D offset.)

A third item to check is normal-mode rejection. Sometimes, what at first appears to be noise is caused by 50 or 60 Hz differential mode signals on the input voltage. Either increase the input filter time-constant, or set the clock frequency so the integration period is an integer multiple of the power line frequency.

A related problem is stray pickup of 50/60 Hz signals in the

analog section of the A/D's external circuitry. When the observed noise varies in a cyclic fashion as the input voltage is raised, consider it a symptom of stray pickup in the analog integrator section.

This occurs because the input voltage determines the duration of the deintegrate mode, and therefore also determines the amount of 50/60 Hz normal mode rejection. The A/D noise will be lowest when the deintegrate cycle is an integer number of line cycles. Conversely, the noise will be highest when the deintegrate cycle is an odd number of half cycles of the line frequency.

The most sensitive node is the junction of the integrator resistor and the integrator capacitor. The auto-zero capacitor is a potential point for stray coupling in many analog-to-digital converters. Stray pickup by these sensitive nodes can be best avoided by keeping connections in this area short and surrounding these components with a guard trace connected to the integrator output.

Nonlinearity Woes

Very poor linearity near full scale is typically caused by satu-

ration of the integrator output stage. Increase the integrator resistor value if the integrator output voltage swings within one volt of either supply rail with positive and negative full-scale inputs. Another potential cause of gross nonlinearity is excessive current draw from the buffer or integrator.

Nonlinearity errors of a couple of counts are usually the result of dielectric absorption in the integrator capacitor. The best test for dielectric absorption is to try a Teflon™ capacitor and see if this cures the problem. Also, do not exceed the input common-mode voltage range of the A/D. For best nonlinearity, keep the input voltage at least 1.5 volts above V₋ and at least one volt below V₊.

Rollover Error

Rollover error is the difference in A/D readings for equal positive and negative voltages near full scale (Figure 5). An example is the difference in the readings on a multimeter when you interchange the input leads. Rollover error can be caused by either a difference in offset for positive and negative voltages or by a difference in gain for these voltages.

The gain error is very com-

TABLE OF SWITCH SETTINGS FOR A/D TEST CIRCUIT

	S1	S2	S3	S4	S5	S6	S7	Input Voltage	Measure
Zero Reading	X	X	O	—	—	—	O	—	Display should read + 0000 or -0000
Ratiometer Error	O	X	X	O	—	X	O	—	Display reads 9998 to 10,000
Rollover Error	O	X	O	O	—	O	±	≈199mV	Rollover error is difference in reading as S7 reverses the input voltage polarity
In Hi Input Leakage	O	X	O	X	—	O	O	—	Leakage in pA = reading ÷ 10
In Lo Input Leakage	O	O	O	O	X	O	O	—	Leakage in pA = $\frac{\text{reading}}{10}$
Common Mode Rejection Ratio	X	O	O	O	—	O	±	V _{CM}	Display should read ±0000 for V _{CM} < 3V
Linearity	O	X	O	O	—	—	±	O to full scale in 0.1FS increments	Measure input V w/ 5½ digit meter compare w/ displayed reading
Zero Code width	O	X	O	O	—	O	±	≈95uV	Find ±0009 to ±0010 transition
Noise	O	X	O	O	—	—	±	Near 0V and full scale	Measure width of transition band where display shows two adjacent readings

X = Closed O = Open — = Don't care

mon, with stray capacitance on the reference capacitor terminals being the most common cause of poor rollover performance. Test for stray capacitance by increasing the reference capacitor value by a factor of 10. If rollover is significantly reduced, then stray capacitance between the reference capacitor and ground is the culprit. Common-mode errors, which offset the entire transfer curve in one direction, will also cause a rollover error.

Input bias current can cause rollover problems when the input source impedance is very high. The ICL7129A uses an input chopping technique to reduce the noise level. This chopping, however, increases the input bias current to about 8 picoamps. If the input source impedance is one Megohm, this small bias current will cause an offset of 8 microvolts, or 0.8 count. If you can't lower the source impedance or add a buffer stage, you may have to use the non-chopped ICL7129, which reduces bias current to 0.1 picoamps while increasing noise level slightly.

Other possible rollover error sources are reference capacitor leakage and low integrator gain in the A/D. You can prevent stray leakage into the reference capacitor by using wide spacings between the reference capacitor terminals and any other circuitry. Guarding these terminals, however, is not recommended, since this will increase the stray capacitance and aggravate rollover problems. At temperatures above 70 degrees C, increase the value of the reference capacitor to minimize the effect of the internal leakage at the A/D reference capacitor input terminals.

A non-zero reading with zero input is rarely seen in the ICL7129A but is sometimes observed in earlier generations of

INTEGRATED CIRCUITS MAGAZINE

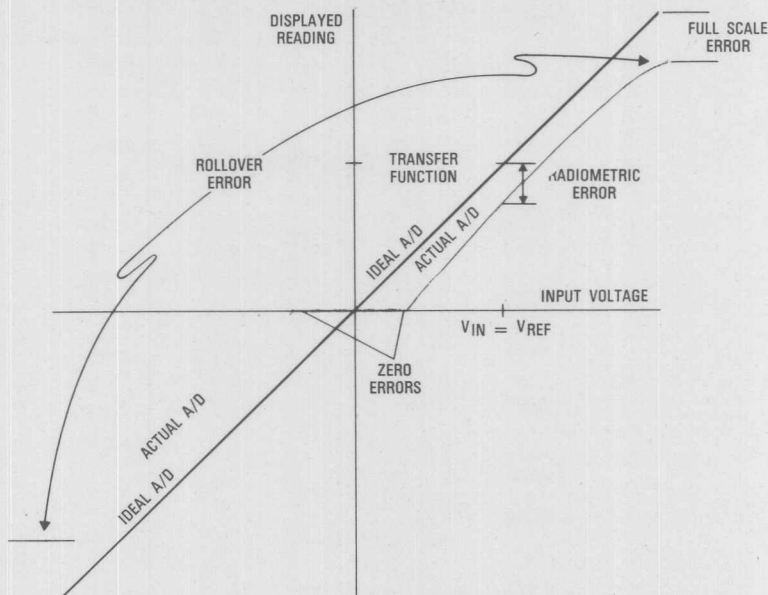


Fig. 5. Error terms of the Intersil ICL7129A are shown here greatly exaggerated. The deviation from a best-fit straight line is the non-linearity error. The difference in displayed readings for equal positive and negative inputs is the rollover error. The deviation from the ideal reading of 10,000 when the reference voltage is applied to the input is the ratiometric error.

A/Ds. You can often trace this problem back to a common-mode voltage between analog ground (or common) and the low (inverting) input terminal of the converter. Connect these two points together directly whenever possible. In all cases, keep the input-low terminal within 2 volts of analog ground and maintain at least a 2-volt margin from both power supply rails.

Single-supply Operation

Integrating A/Ds can be operated from a single 5-volt supply if you observe several precautions. Keep the input-common and input-low terminals centered between V^+ and ground. It may also be necessary to increase the value of the integrating capacitor, so that the integrator swings to about 1 volt from V^+ and ground when full-

scale inputs are applied. In addition, you should limit the full-scale input to 1 volt and increase the value of the auto-zero capacitor by a factor of four, to reduce noise.

The circuit shown in Figure 1 is suitable for virtually all integrating A/Ds. Most of these converters use an autozero capacitor in series with the integrator input, but this does not change the test procedures. The input voltage, however, must correspond with the full-scale voltage actually being used. The only other significant difference among the commonly available integrating A/Ds is whether they are intended for single-supply or dual-supply operation. For dual-supply converters, separate grounds for the digital section and the analog section are essential. ■

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Digital Feedthrough - This occurs when logic transitions on a DAC's digital inputs generate noise on its analog output. Proper board layout and grounding can reduce this, but some amount of feedthrough will always occur through the DAC itself. To date, no effective means has been found to eliminate this in a single chip. Some application solutions are:

1) Ignore it. In systems not using latches or a data bus, this may be acceptable. Digital noise will occur only when the DAC's output is being changed and can be lumped together with settling errors.

2) Use external data latches. Bus logic transitions from other activity do not reach the DAC input pins at all. DACs containing extra digital buffers may of course be redundant in this case.

3) Use a second "quiet" data bus. If extra I/O lines are available, then the DAC can be programmed from a dedicated bus that doesn't move unless the DAC is receiving data. A DAC with a serial data format, such as the MAX543, ties up the fewest data lines.

Wideband Noise - In most CMOS DAC circuits, the reference and output amplifier are the most frequent sources of objectionable wideband noise. Current-output CMOS DACs (like the MX7541A) are passive in the signal path and generate almost no noise of their own. Voltage-output CMOS DACs (like MX7226) have internal output amplifiers which do generate noise.

A simple way to determine the source of wideband DAC noise is to note how its amplitude changes with DAC code. If the noise is proportional to input code then reference noise is most likely the cause. With DC references, filtering can be added to the reference input to reduce this. If the noise is code-independent then the output amplifier is to blame.

DAC Output Settling - If the settling performance of a DAC circuit is less than expected, carefully observe the power supply behavior AT THE POWER SUPPLY PINS of the DAC and output amplifier. Analog output signals will rarely settle to any reasonable accuracy (1% or better) until supply glitches have decayed. Supply transients are suppressed most effectively when bypass capacitors are placed as close to the DAC and amplifier as physical limits permit. See also the "A/D, D/A Question/Answer Primer" at the front of the "Analog to Digital Converters" section.

Full Scale Adjustment and External Feedback Resistors - CMOS current-output multiplying DACs (MX7541A, MX7545, MAX543, etc.) owe excellent stability and linearity to the fact that their on-chip resistors are well matched. Unfortunately excellent matching does not also mean that the absolute value of these resistors is particularly accurate, or stable with temperature. This is why a feedback resistor, for connection to an external op amp, is also provided on chip -- so it tracks the resistors in the DAC. Therefore, in the typical application of these devices, absolute resistance has literally no effect on DAC

output accuracy because changes in the DAC resistance are matched by the on-chip feedback resistor. The output is then not affected by part-to-part, or temperature related, resistance changes.

Some DAC applications, particularly those with full scale trims, get into trouble because they rely on some level of absolute accuracy in the DAC reference input and feedback resistance. If the adjustments have limited range, accuracy and drift are only negligibly affected, but as the span of the adjustment is widened, the adverse effects can then become significant.

Figure 4-1 shows a typical "safe" adjustment scheme for a 12-bit DAC. A 100Ω resistor (R2) is connected in series with the DAC's internal feedback resistor at RFB. This increases the DAC gain by small amount so that the 200Ω trim pot (R1) at VREF has adjustment range both above and below the DAC's untrimmed full-scale value. The absolute resistance at RFB and VREF is nominally 11kΩ, but it can range from 7kΩ to 25kΩ and has a typical temperature coefficient of -300ppm/°C (not to be confused with the DAC's untrimmed gain drift of <10ppm/°C). This resistance determines the trim range of R1. At 11kΩ, this allows a ±0.9% full scale adjustment, but over the specified resistance of 7kΩ to 25kΩ, this changes significantly. At 25kΩ, the trim range lowers to ±0.4%.

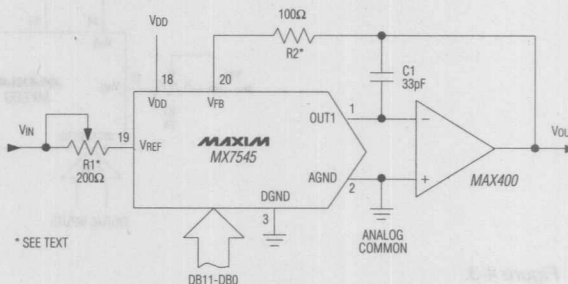


Figure 4-1.

If the trim resistances are small compared to the DAC resistance, the effect of tracking mismatch on temperature drift is minimal. The 100Ω mismatch between the reference and feedback resistance, 7kΩ, the minimum DAC resistance no longer tracks over temperature. Assuming ±300ppm/°C DAC resistor drift and ±100ppm/°C trim pot drift, the additional output drift is:

$$(100/7000) (300+100) = 5.7 \text{ (ppm/°C)}$$

If we attempt, however, to trim ±10% of the full scale range with the highest DAC resistance (25kΩ), R2 must be 1.25kΩ and R1 must be 2.5kΩ. With these values the above calculation becomes:

$$(2500/7000) (300+100) = 143 \text{ (ppm/°C)}$$

This amounts to almost 0.6 LSB/°C of gain drift at 12 bits. As can be seen from the equations, even if 0ppm/°C resistors are used for R1 and R2 instead of 100ppm/°C, the drift only marginally improves. Therefore

any wide-range trim scheme that involves adding resistance in series with VREF or RFB on a CMOS multiplying DAC, should be checked in the above manner.

Bipolar DAC Operation (4-Quadrant Multiplication)

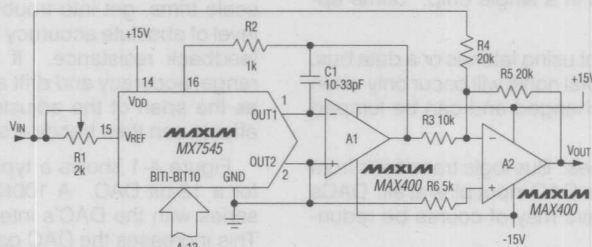


Figure 4-2.

Unipolar Binary Operation (2-Quadrant Multiplication)

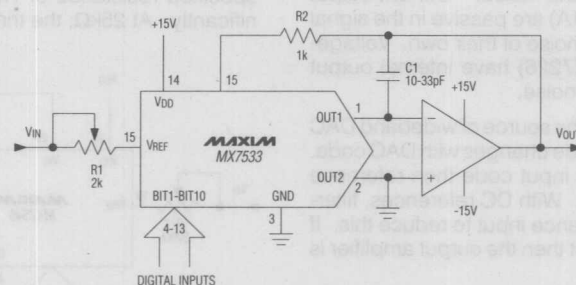


Figure 4-3.

Digitally Controlled Op Amp Gain

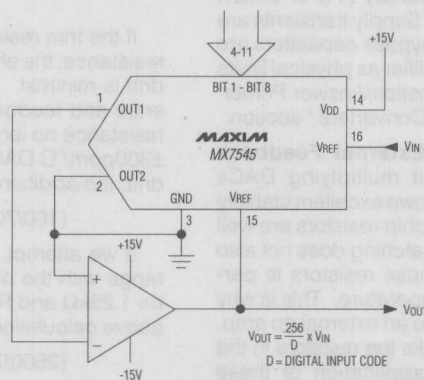


Figure 4-4.

Single Supply Operation

The MX7528/MX7628 R-2R ladder termination resistors are internally connected to AGND. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between VDD and DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the stable matched impedances of the DAC A and DAC B reference inputs. Current flows through the DAC A and DAC B reference inputs and through the DAC R-2R ladders into R1, and R2. DAC codes from 00000000 to 11111111 adjust the analog output voltages from +5V to +8V in 11.7mV steps.

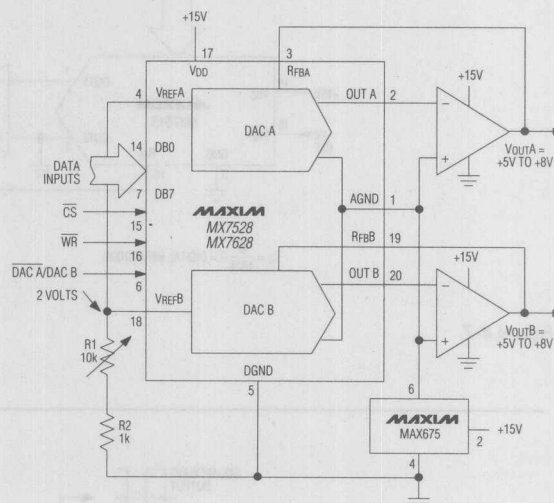


Figure 4-5.

MX7224 Bipolar Output

The DAC output may be configured for bipolar operation using the circuit in Figure 4-6. Only one op-amp and two resistors are required. With $R1 = R2$:

$$V_{OUT} = V_{REF} (2D - 1)$$

where D is a fractional representation of the digital word in the DAC register.

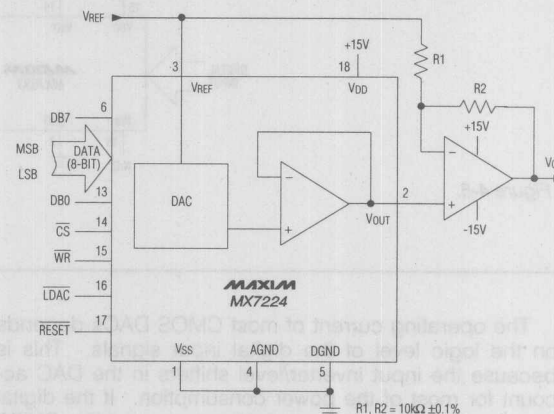


Figure 4-6.

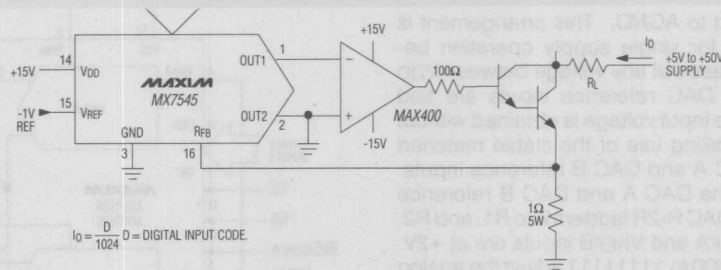


Figure 4-7.

Programmable Function Generator

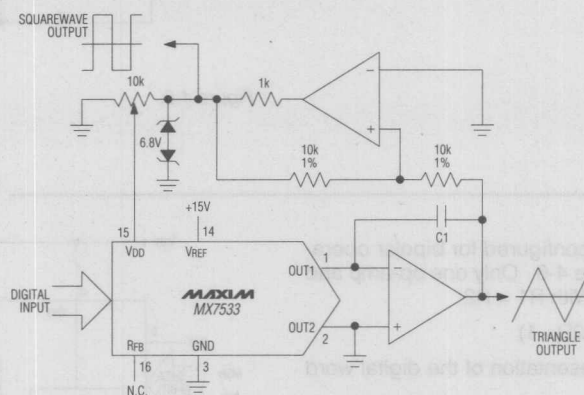


Figure 4-8.

Reducing CMOS DAC Supply Current

The operating current of most CMOS DACs depends on the logic level of the digital input signals. This is because the input inverter/level shifters in the DAC account for most of the power consumption. If the digital inputs are made to swing from VDD to ground (i.e. CMOS logic levels) rather than to TTL levels, the supply current is typically cut by a factor of 100 or more. When the DAC output is changing, the supply must still supply 5 to 10mA for about 20ns, independent of input logic level, but this is usually a small fraction of the total operating time.

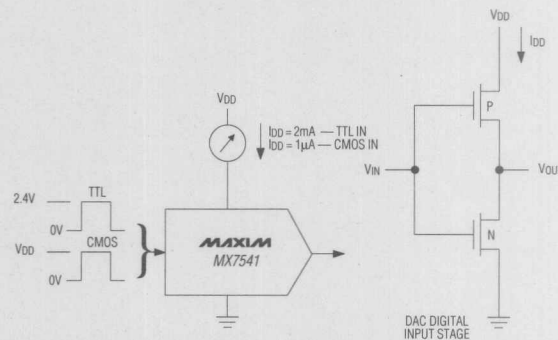


Figure 4-9.

The MX7533 or other current output CMOS DAC may be connected as a voltage output DAC as shown. OUT1 is connected to the external reference and OUT2 is grounded. VREF, now the DAC output, is a voltage source with a constant output resistance, nominally 10k Ω . In most circuits this output is buffered with an op-amp.

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted. The reference input (voltage at OUT1) must always be positive and is limited to no more than 3.5V when VDD is 15V. If the reference voltage is greater than 3.5V, or VDD is reduced, linearity is degraded. If a larger output voltage is needed, the output buffer can be connected for noninverting gain.

Some newer CMOS DAC's have voltage outputs included and do not require special connections for single supply operation. These are:

PART	V SUPPLY	DESCRIPTION
MX7224	+12 TO 15V	CMOS 8 bit, voltage out
MX7225	+12 TO 15V	CMOS quad 8 bit, voltage out
MX7226	+12 TO 15V	CMOS quad 8 bit, voltage out
MX7228	+5V TO 15V	CMOS octal 8 bit, voltage out

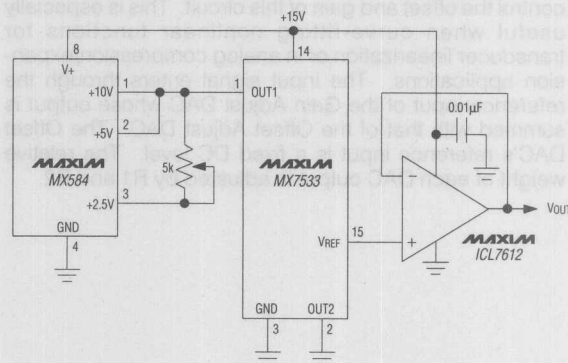


Figure 4-10. Voltage Mode Operation

Digital Calibration and Threshold Selection

The circuit is used to discriminate "light" and "dark" conditions in photo-sensing applications where the light levels are better described as "bright" or "dim". Applications include tachometers, motion sensing, automatic readers, and liquid clarity examination.

A calibration "bright" light is applied while the DAC is digitally ramped. The count of the ramp at the trip point is then the high calibration point. Similarly, a "dim" calibration light is applied and a low calibration point is determined. The trip threshold is placed between the two calibration points, and the μ P sets this value up on the DAC inputs. Continuously varying light levels are judged "light" or "dark" according to whether or not they exceed this level.

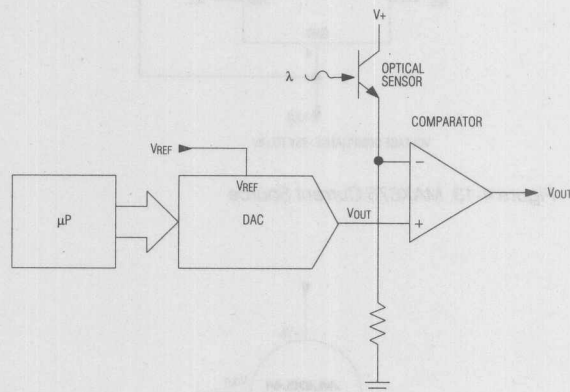


Figure 4-11.

Two voltage-output DACs (or a dual DAC) digitally control the offset and gain of this circuit. This is especially useful when curve-fitting nonlinear functions for transducer linearization or in analog compression/expansion applications. The input signal enters through the reference input of the Gain Adjust DAC whose output is summed with that of the Offset Adjust DAC. The Offset DAC's reference input is a fixed DC level. The relative weight of each DAC output is adjusted by R1 and R2.

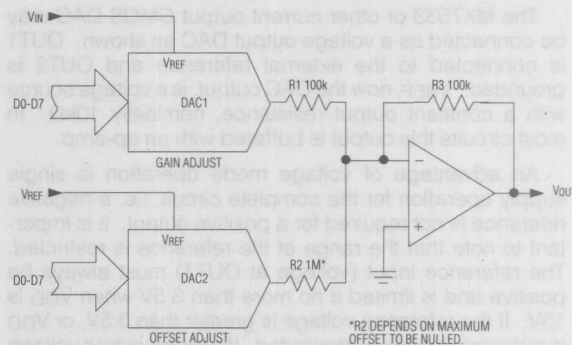


Figure 4-12.

Current Source/Limiter Circuits

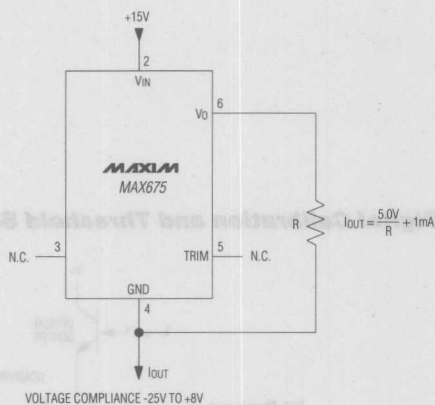


Figure 4-13. MAX675 Current Source

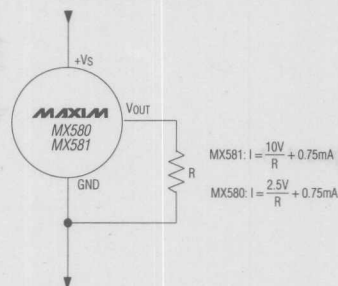


Figure 4-14. Two-Component Precision Current Limiter

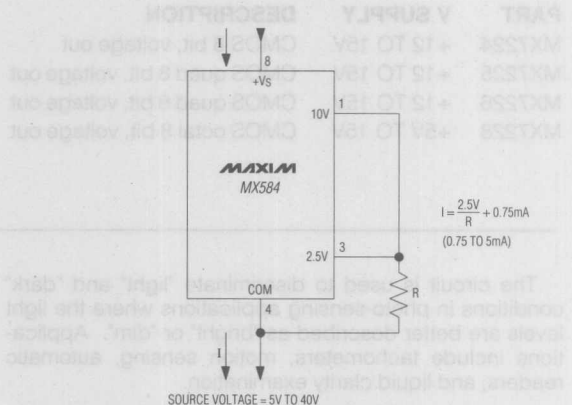


Figure 4-15. Precision 2 Terminal Current Limiter

A PNP power transistor, or Darlington, is easily connected to the MX584 to greatly increase its output current. The circuit in Figure 4-16 provides a +10V output at up to 4 Amps. If the load has a significant capacitive com-

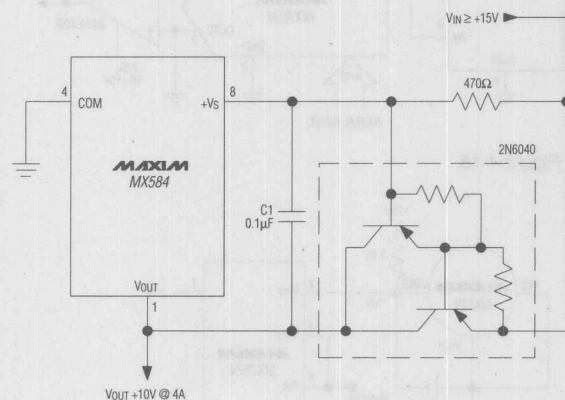


Figure 4-16. High Current Precision Supply

ponent, C1 should be added. If the load is purely resistive, high frequency supply rejection is improved without C1. An NPN output transistor or Darlington can also be used to boost output current as shown in Figure 4-17.

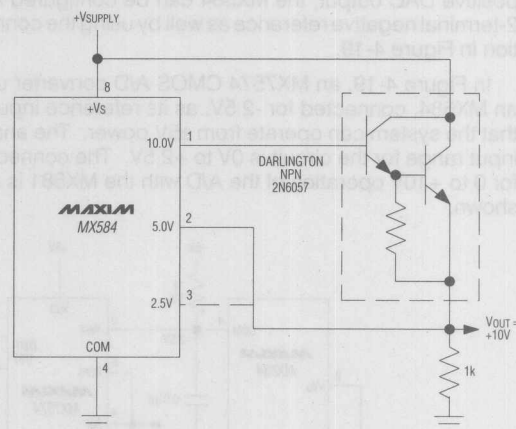


Figure 4-17. NPN Output Current Booster

The MX584 is well suited for use with a wide variety of D-to-A converters, especially CMOS DACs. Figure 4-18 shows a circuit in which an MX7533 10 bit DAC has an output of 0 to -5V when using a +5V reference. For a positive DAC output, the MX584 can be configured as a 2-terminal negative reference as well by using the connection in Figure 4-19.

In Figure 4-19, an MX7574 CMOS A/D converter uses an MX584, connected for -2.5V, as its reference input so that the system can operate from $\pm 5V$ power. The analog input range for the circuit is 0V to +2.5V. The connection for 0 to +10V operation of the A/D with the MX581 is also shown.

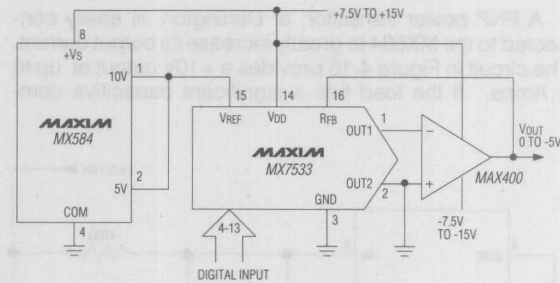


Figure 4-18.

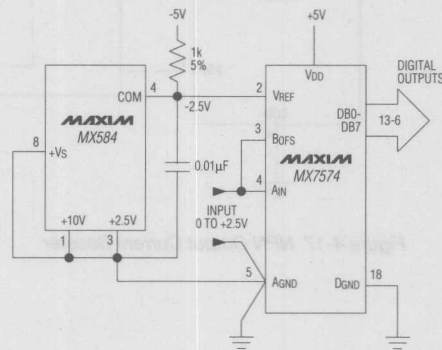
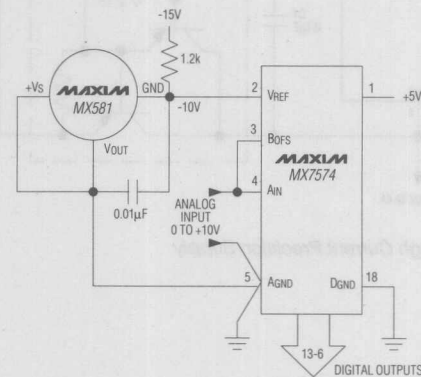


Figure 4-19. Negative -2.5V and -10V Reference for a CMOS A/D



Negative and Bipolar Output Reference Circuits

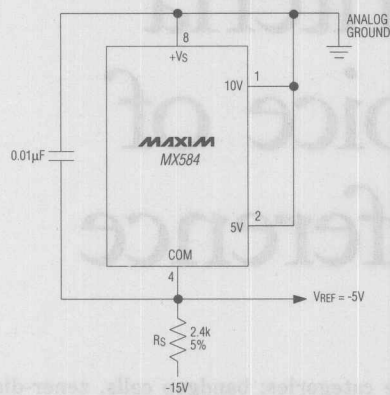


Figure 4-20. Two-Terminal -5 Volt Reference

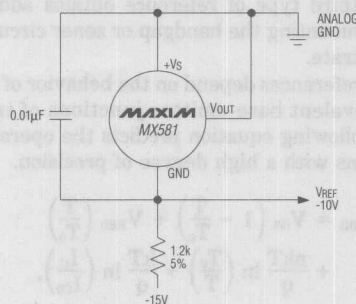


Figure 4-21. Two-Terminal -10 Volt Reference

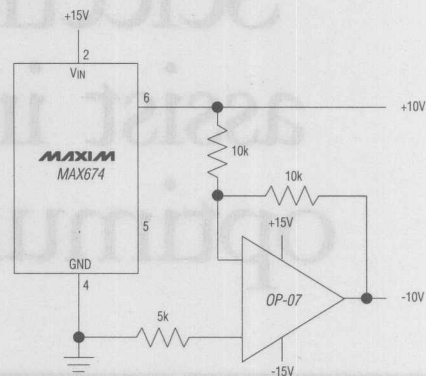


Figure 4-22. $\pm 10V$ Reference

When using the 2-terminal connection, the load and the bias resistor must be selected so that the current flowing in the reference is maintained between 1mA and 5mA. The operating temperature range for this connection is limited to -55° to $+85^{\circ}\text{C}$.

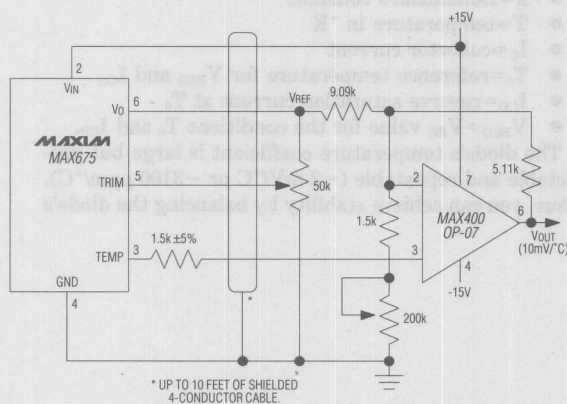


Figure 4-23. Precision Temperature Transducer with Remote Sensor

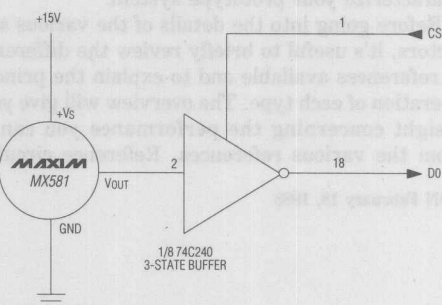


Figure 4-24. Microprocessor Reference Interface

Selection criteria assist in choice of optimum reference

It's not always easy to select the most suitable precision voltage reference for your application. These devices often require parametric and economic tradeoffs. Further, parameters that are crucial in some systems are missing from or presented unclearly in many data sheets. An overview of selection criteria can help you make the choice.

Ron Knapp, Maxim Integrated Products

In choosing a precision voltage reference, you should look beyond initial accuracy, temperature coefficient (TC), and cost. Other factors that determine the suitability of a reference for your application are the device's power dissipation, noise, long-term stability, package size, ease of use, TC linearity, and the manufacturer's definition of TC. Familiarity with these selection criteria will help you avoid unpleasant surprises when you characterize your prototype system.

Before going into the details of the various selection factors, it's useful to briefly review the different types of references available and to explain the principles of operation of each type. The overview will give you some insight concerning the performance you can expect from the various references. Reference circuits com-

prise three categories: bandgap cells, zener-diode-based references, and heated-substrate types. Most voltage references fall into the first two categories and derive their fixed output from a bandgap cell or a zener diode. The third type of reference obtains additional stability by mounting the bandgap or zener circuit on a heated substrate.

Bandgap references depend on the behavior of diodes (or the equivalent base-emitter junctions of transistors). The following equation predicts the operation of such junctions with a high degree of precision.

$$V_{BE} = V_{G0} \left(1 - \frac{T}{T_0} \right) + V_{BE0} \left(\frac{T}{T_0} \right) + \frac{nkT}{q} \ln \left(\frac{T_0}{T} \right) + \frac{kT}{q} \ln \left(\frac{I_C}{I_{C0}} \right),$$

where

- V_{G0} = the extrapolated bandgap voltage (about 1.2V) at 0°K
- n = process-dependent constant; value 1.5 to 3
- q = charge of an electron
- k = Boltzmann's constant
- T = temperature in °K
- I_C = collector current
- T_0 = reference temperature for V_{BE0} and I_{C0}
- I_{C0} = reverse saturation current at T_0
- $V_{BE0} = V_{BE}$ value for the conditions T_0 and I_{C0} .

The diode's temperature coefficient is large but predictable and repeatable (−2 mV/°C or −3100 ppm/°C). Thus, you can achieve stability by balancing the diode's

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The V_{BE} equation's third and fourth non-linear terms limit the performance of bandgap references by making a flat voltage/temperature response impossible.

TC with a TC of equal magnitude and opposite sign. Such a TC exists for the difference between the forward voltages of two diode junctions operating at different current densities. Because the ratio of mismatch governs the TC's value, the bandgap circuit is compatible with good IC design—parameter values should depend on accurate ratios based on layout geometry, rather than on absolute quantities that are difficult to control.

You can calculate the desired difference voltage (ΔV_{BE}) with high predictability, directly from the diode equation

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{J_1}{J_2} \right),$$

where J_1/J_2 is the ratio of current densities. To obtain zero TC, you add the expression for V_{BE} to the one for ΔV_{BE} , differentiate the sum with respect to temperature (T), and set this quantity equal to zero. The result is

$$V_{G0} = V_{BE0} + \frac{kT}{q} \ln \left(\frac{J_1}{J_2} \right).$$

Solving this equation for the J_1/J_2 ratio tells you that an approximate 8:1 ratio gives the best result (a near zero TC). Scaling the transistor areas gives an IC designer accurate control of this ratio.

In a basic bandgap circuit (Fig 1), V_{BE} is the base-

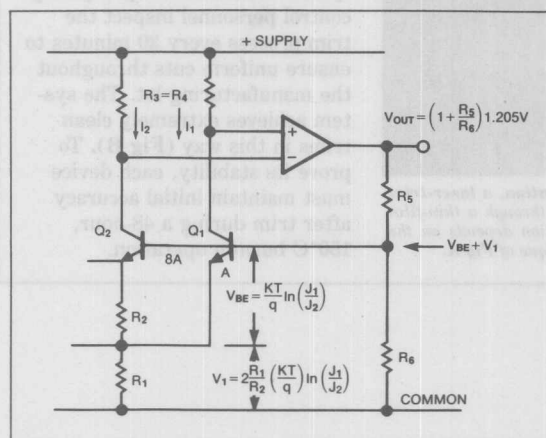


Fig 1—A bandgap voltage reference generates the sum ($V_{BE} + V_1$), in which the two voltages have equal and opposite temperature coefficients. The amplifier then raises the sum to a more convenient voltage level.

emitter voltage of Q_1 , and ΔV_{BE} appears across R_2 . The ratio of R_1 and R_2 scale ΔV_{BE} to a voltage (V_1) whose TC cancels the TC of V_{BE} . The amplifier then raises the 1.2V sum of V_1 and V_{BE} (the bandgap-cell voltage) to a higher level at V_{OUT} : usually 2.5 to 10V. Unfortunately, the amplifier multiplies noise as well. A 10V scaled output, for example, increases the bandgap cell's noise voltage by an approximate factor of 8 ($10 \div 1.2$).

Commonly available bandgap-reference voltages are 10, 5, 2.5V, and the bandgap-cell voltage itself, 1.23V. Typical TCs range from 5 to 50 ppm/°C. The V_{BE} equation's higher-order, logarithmic third and fourth terms limit the performance of these references by making a flat voltage-temperature response impossible. What's more, some of the equation's coefficients are process-dependent—particularly n , which is related to the carrier mobility of dopant in the silicon. The quantity n poses a problem because you cannot easily determine its value by making electrical measurements during production.

Because most bandgap references are constructed in silicon monolithic form, they are relatively inexpensive (\$3 to \$20). Many designs employ curvature correction to compensate for the logarithmic nonlinearity in the TC, but none offer an exact cancellation.

Zeners have rock-bottom TCs

The second type of voltage reference—based on a zener diode—achieves TCs as low as ± 1 ppm/°C. Zener diodes have a positive or negative TC, depending pri-

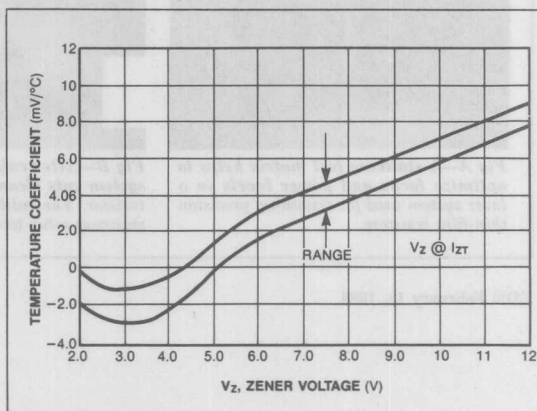


Fig 2—Zener diodes produce a zero-TC voltage near 5V—the level for which the mechanisms of negative-TC field-emission breakdown and positive-TC avalanche breakdown are in balance. However, the zero-TC ideal is difficult to achieve on a production basis.

which dominates below 5V and produces a negative TC, and avalanche breakdown, which occurs above 5V and yields a positive TC. Although complex and difficult to quantify, these breakdown mechanisms should be in balance at approximately 5V, yielding a near-zero TC. Tests corroborate this contention (Fig 2).

Unfortunately, 5V zener diodes exhibiting the utopian zero TC are difficult to produce. The problem is that the negative TC breakdown mechanism is flukey and difficult to reproduce consistently in production. The positive TC breakdown, on the other hand, is predictable and eminently repeatable for devices using routine semiconductor-production processes. Another charac-

because of the difficulty of producing a zero-TC zener diode that depends purely on breakdown mechanisms, it's evident that the TC of a zener-diode reference should not depend solely on the absolute zener breakdown voltage. A class of zener diodes, called TC zeners, takes a compensatory approach by balancing the negative TC of a forward-biased diode ($-2 \text{ mV}/^\circ\text{C}$) with the equal and opposite TC of a 5.6V zener diode. The output voltage is therefore 6.3V ($0.7\text{V}+5.6\text{V}$). These references offer 5- to 100-ppm/ $^\circ\text{C}$ TCs and require operating currents from 0.5 to 7.5 mA. You must maintain the specified operating current to obtain the guaranteed TC.

Precision references need laser trimming

To achieve accuracies as tight as $\pm 0.01\%$ in precision references, manufacturers use laser-trimmed thin-film resistors. Diffused resistors embedded within silicon exhibit not only hysteresis, but also high TC, poor TC matching, large voltage coefficients, and poor stability. Thin-film resistors, deposited on the chip's surface, are found in such voltage references as the REF01, AD581, AD2700, and the MAX670.

The secret to the precision references' accuracy is to trim

the thin-film resistors by laser before attaching a lid to the package. This critical operation determines a reference's initial accuracy and its long-term stability. Fuse-link blowing and resistor-link trimming are alternative schemes for trimming the absolute voltage, but the chip area required with these methods makes them prohibitively expensive for tight-tolerance adjustments.

Thick-film resistors have insufficient stability for use in precision references; therefore, hy-

brid products such as the MAX670, AD2700, and AD2710 include TaN (tantalum nitride) or NiCr (nichrome) thin-film resistors, sputtered on a ceramic substrate of 99.6% alumina (Al_2O_3). Before trimming each lot of references, the manufacturer determines the optimum settings for laser power and focus by executing a test matrix of experimental laser cuts.

For each power setting, the system makes a staircase trim pattern in which each right-angle turn marks an additional increment of focus (Fig A). After completion of the focusing and system-calibration steps, quality-control personnel inspect the trim process every 30 minutes to ensure uniform cuts throughout the manufacturing lot. The system achieves extremely clean trims in this way (Fig B). To prove its stability, each device must maintain initial accuracy after trim during a 48-hour, 150°C burn-in operation.

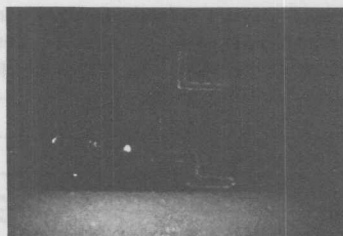


Fig A—A staircase test matrix helps to optimize focus and power levels in a laser system used for trimming precision thin-film resistors.

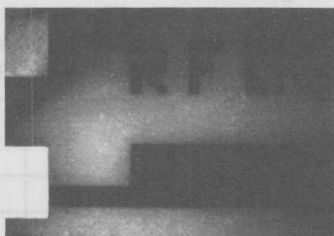


Fig B—After calibration, a laser-trim system cuts cleanly through a thin-film resistor. The calibration depends on the staircase setup technique of Fig A.

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You can easily achieve a 1-ppm/°C TC by mounting a zener-reference circuit of reasonably low TC on a heated substrate.

The AD2700 and MAX670 series of hybrid references, for example, use a 1N827 zener diode—chosen for low noise, low dynamic impedance (10Ω max), and good TC linearity. (Why use a hybrid? Fabrication of these TC zener references involves a specialized process, involving extra steps not always available in a standard bipolar process.) The products' initial 10-ppm/°C TC is that of the zener diode. Active laser trimming then lowers the TC by adjusting the zener-diode current, thereby creating additional 3- and 1-ppm/°C product grades (see box, "Precision references need laser trimming").

The manufacturer calculates the required zener current using actual TC values, obtained through oven tests on unsealed devices. Note that the amplifier in Fig 3 supplies current to the zener, which in turn supplies an input voltage to the amplifier. To ensure circuit startup, R_4 supplies current to the zener and the amplifier uses ground as its negative supply, thereby eliminating $V_{OUT}=0V$ as an unwanted stable state. Note that the amplifier in a zener reference contributes less output noise than does the amplifier in a bandgap reference, because the zener voltage requires less amplification.

Heater trades P_D for stability

The third type of reference, based on either a bandgap or zener voltage, uses a local heater to maintain the substrate at a constant temperature, usually 10 or 15 degrees above the upper limit of the operating

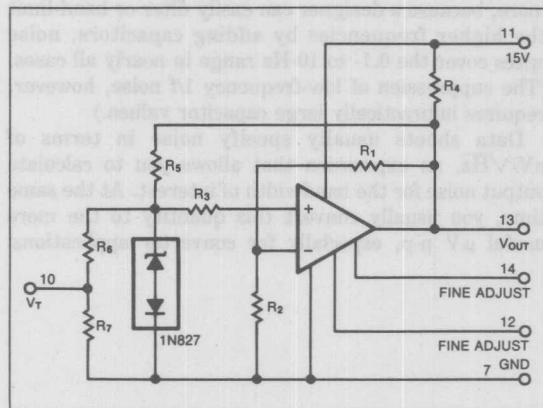


Fig 3—The amplifier in this zener-diode reference bootstraps the zener voltage by delivering current to the zener while the zener delivers voltage to the amplifier. R_4 provides start-up current to the zener.

range. If the circuit's TC is reasonably low (20 to 30 ppm/°C), such a reference can easily achieve a TC of 1 ppm/°C. The disadvantage is power dissipation—an LM199 at -55°C, for example, requires as much as 28 mA at 15V for the heater alone.

Also, the LM199's output voltage stabilizes at 1 ppm/°C but the initial accuracy is only $\pm 5\%$. To meet the $\pm 0.1\%$ or $\pm 0.01\%$ tolerances required in data-converter applications, therefore, you must add a precision op amp and scaling resistors and then cope with these components' additional cost and error contributions. The proper evaluation of a reference application involves these issues as well as many of the following ones, which are not always covered explicitly in the data sheet.

Confusion surrounding the specification of temperature coefficient, for instance, is partly a matter of definition. Two definitions are popular. In the "box" method, V_{OUT} for an in-spec device must remain within a rectangle formed by T_{MIN} , T_{MAX} , and the maximum specified ΔV_{OUT} (Fig 4). ΔV_{OUT} is the product of the nominal output voltage (V_{NOM}), the specified TC, and the operating-temperature range. For the AD2700L,

$$\begin{aligned}\Delta V_{OUT} &= V_{NOM} (TC) (T_{MAX} - T_{MIN}) \\ &= 10V(3 \text{ ppm/}^\circ\text{C}) [85 - (-25)^\circ\text{C}] \\ &= 3.3 \text{ mV.}\end{aligned}$$

In other words, V_{OUT} will change no more than ± 3.3 mV between any two temperatures in the operating range. This maximum change, added to the ± 2.5 -mV initial-accuracy spec, produces a total error band of 5.8 mV above and below the nominal V_{OUT} (10V).

The "butterfly" method, on the other hand, refers everything to 25°C and allows the manufacturer to use

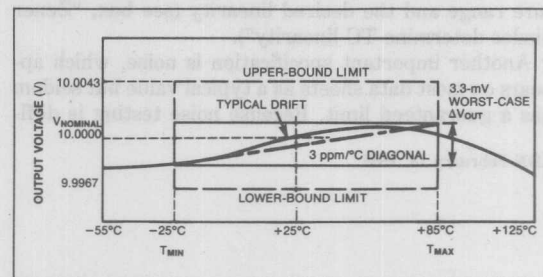


Fig 4—In the "box method" of specifying TC, the operating-temperature range and the maximum allowed change in V_{OUT} form the sides of a rectangle, and the slope of the rectangle's diagonal becomes the TC.

different TCs in determining the error bands at temperatures above and below 25°C (Fig 5). The AD2710K, for example, specs a change of ± 0.9 mV over the 25 to 70°C range ($10\text{V} \times 2 \text{ ppm}/^\circ\text{C} \times (70 - 25)^\circ\text{C}$). You must add to this the initial tolerance of ± 1 mV at 25°C, resulting in a maximum possible error of ± 1.9 mV at T_{MAX} (70°C).

Such systems as DVMs and data-acquisition instrumentation often use the box method for specifying total error, because users aren't likely to calculate accuracy using the TC specs. This approach has a disadvantage—the whole 3.3-mV error change in the example of Fig 4 could occur between, say, 25 and 70°C, yielding an effective TC of 7.33 ppm/°C, which exceeds the maximum specified TC (3 ppm/°C). A worst-case analysis over temperature, however, must allow for this much change anyway, regardless of where it occurs in the operating-temperature range.

Because temperature testing plus the reading and recording of data are costly, manufacturers usually base TC specs on only a few data points. These should include at least 25°C and the endpoints (T_{MIN} and T_{MAX}). Using the endpoints alone, for example, can make the reference appear better than it actually is if the TC curve is symmetrical and parabolic.

You should avoid using "typical" specs for TC and absolute accuracy; only tested and guaranteed limits for minimum and maximum have meaning. A data sheet should also identify the temperatures used in the calculation of the device's TC. The AD2700L data sheet, for instance, lists 25°C plus the endpoints (–25 and 85°C). The AD2700U data sheet lists these three as well as the extended endpoints of –55 and 125°C.

Correction yields S curve

Although voltage-reference data sheets seldom specify TC linearity, the characteristic curves for V_{OUT} over temperature contain the most useful TC-linearity information that a manufacturer can provide. For bandgap references these curves are parabolic or S-shaped (Fig 6), depending, among other factors, on whether the device includes a linearity-correction circuit. The TC linearity of zener-based references depends mainly on the zener diode, and the reference will include one of two diode types, depending on the intended temperature range and the desired linearity (see box, "Zener diodes determine TC linearity").

Another important specification is noise, which appears on most data sheets as a typical value but seldom has a guaranteed limit. Because noise testing is diffi-

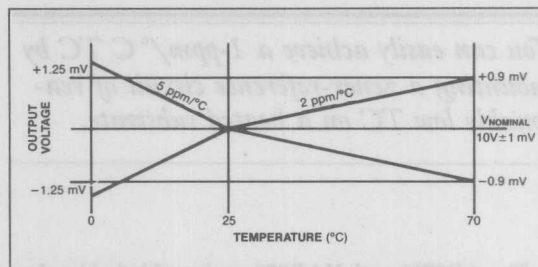


Fig 5—The "butterfly" method of TC specification normalizes the variation of V_{OUT} with respect to 25°C. You then extend wing-shaped error bands to the operating-temperature extremes.

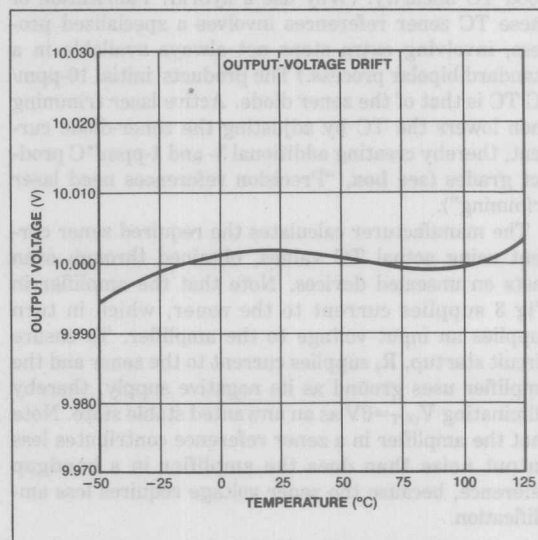


Fig 6—The AD581's V_{OUT} -vs-temperature characteristic has an S-shaped curve. This characteristic is typical for bandgap references that include correction circuits for TC linearity.

cult, manufacturers usually guarantee maximum values by performing sample testing only, if that. What's more, because a designer can easily filter or band-limit the higher frequencies by adding capacitors, noise specs cover the 0.1- to 10-Hz range in nearly all cases. (The suppression of low-frequency 1/f noise, however, requires impractically large capacitor values.)

Data sheets usually specify noise in terms of $\text{nV}/\sqrt{\text{Hz}}$, an expression that allows you to calculate output noise for the bandwidth of interest. At the same time, you usually convert this quantity to the more useful μV p-p, especially for converter applications:

Bandgap references usually have a parabolic TC characteristic that assumes an S shape if the device includes circuitry to effect linearity correction.

First, multiply $nV/\sqrt{Hz}$ by the square root of the system bandwidth to obtain the noise magnitude in nV rms. Then (assuming the noise has a Gaussian distribution), multiplication by 6 will give you the approximate peak-to-peak noise you can expect for that bandwidth.

Noise measurement is difficult

Lack of equipment is part of the difficulty manufacturers face in measuring noise. For example, Quantec makes a noise tester commonly used for testing op amps and transistors, but that instrument requires a nominal 0V bias for the circuit node under test. Spectrum

analyzers make good noise testers, but not many have the dynamic range and the low noise floor necessary to measure, say, $10\text{-}\mu V$ signals riding on 10V dc. Frequency range is another complication. Spectrum analyzers come in high- or low-frequency models (above or below 100 kHz), so one model doesn't cover the measurement range needed for many applications—0.1 Hz to several megahertz.

You can measure noise directly using a Tektronix storage oscilloscope with a 7A22 plug-in amplifier, which has $10\text{-}\mu V/\text{div}$ sensitivity and selectable lowpass and highpass filters that cover 0.1 Hz to 1 MHz. The

Zener diodes determine TC linearity

The TC linearity for a zener-based voltage reference depends on the type of zener diode in the device. Most hybrid references

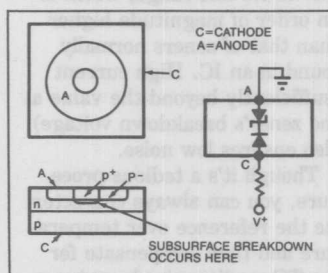


Fig A—Alloy-diffused zener diodes feature a vertical configuration in which a top-surface bond pad forms the anode connection and the die substrate forms the cathode connection.

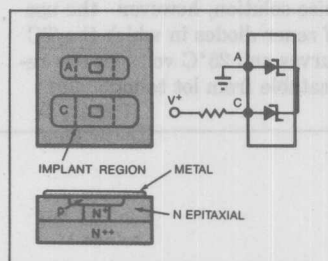


Fig B—The lateral geometry of ion-implanted zener diodes places both diode connections on the top surface of the chip.

include one of two types of TC zener (in die form), and only a few zener manufacturers can guarantee 5- to 10-ppm/ $^{\circ}C$ performance for these products.

One zener type has an alloy-diffused junction in a vertical configuration (Fig A), wherein the anode serves as a bond pad on top of the die and the cathode as the substrate (backside) of the chip.

The other type of zener features an ion implant and lateral geometry (Fig B), and has both connections on top of the chip. For this type, the substrate must float unconnected, because the substrate is the junction of two zener diodes—one operating as a zener in the breakdown mode, and the other operating as an ordinary forward-biased diode. The zener voltage is 5.6V,

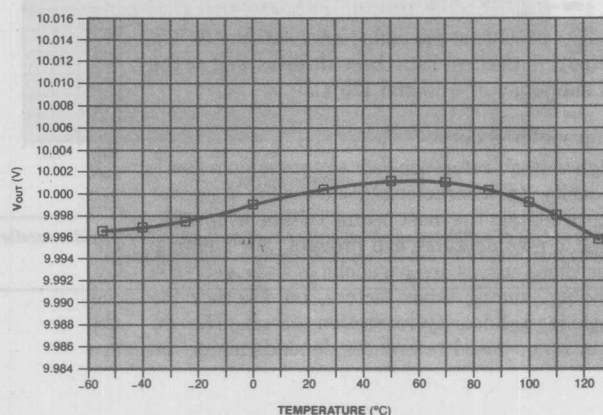


Fig C—An ion-implanted-zener reference such as the AD2700 exhibits a concave-down TC characteristic and better overall linearity than does a diffused-zener type for the range -55 to $+125^{\circ}C$.

lowpass settings don't include 10 Hz, however, and the amplifier's input-voltage limitation may require that you ac-couple the signal. The coupling capacitor then forms a highpass filter of a few hertz that precludes the use of the 0.1-Hz highpass setting.

For a more convenient method of noise testing with a storage oscilloscope, you use a low-noise op amp configured for a gain of 100, a 0.1-Hz highpass input filter, and a 10-Hz lowpass output filter (Fig 7). The gain boosts 10- μ V signals to 1 mV—within the range of most oscilloscopes—and allows use of an OP07A (whose 0.6- μ V p-p max noise contributes less than 60 μ V p-p

noise at the output).

To measure noise, set the scope amplifier's vertical-input coupling to dc. Allow the filter to settle and the reference to warm up (about 30 sec in most cases). Clear the screen in storage mode and set the time base for single-trigger mode at 1 sec/div. Set the scope to save mode or maximum screen persistence and measure the peak-to-peak noise for 10 sec. (Observation for 10 seconds is the accepted method, even though the time constant for 0.1 Hz is only 1.6 sec.) A scope photo based on this technique (Fig 8) shows about 20- μ V p-p noise for the AD581—typical for most bandgap references—

and when operated at the proper current, it produces a TC of 2 mV/ $^{\circ}$ C—a TC equal to and opposite that of the forward-biased diode. For this reason, nearly all temperature-compensated zener diodes have a total voltage of 6.3V (5.6+0.7V). You can create a higher output voltage by connecting multiple forward-biased diodes in series with a higher-voltage zener diode.

Both TC-zener types specify

V_{OUT} as $6.3V \pm 5\%$, but the actual tolerance for ion-implanted types is tighter (typically ± 40 mV, or $\pm 0.6\%$), vs ± 300 mV ($\pm 4.7\%$) for alloy-diffused types. The tighter tolerance of ion-implanted zener diodes allows the reference manufacturer to target gain-resistor values more closely, do less laser trimming, and thereby provide better V_{OUT} stability.

TC linearity is the most no-

ticeable difference between the two zener types. The implanted zener's concave-down curve exhibits better overall linearity from -55 to 125° C (Fig C), but the diffused zener has better TC linearity from 0 to 70° C (Fig D). Both the forward-biased diode and the zener diode contribute to the nonlinearity, and these effects increase at low current.

Accordingly, most TC zeners have operating currents in the 0.5- to 7.5-mA range, which is an order of magnitude higher than that of zeners normally found in an IC. High current (sufficiently beyond the value at the zener's breakdown voltage) also ensures low noise.

Though it's a tedious procedure, you can always characterize the reference over temperature and then compensate for the TC nonlinearity by using a temperature sensor, A/D converter, and software lookup table. The well-controlled ion-implant process offers a compromise solution, however—the use of zener diodes in which the TC curves and 25° C voltages are repeatable from lot to lot.

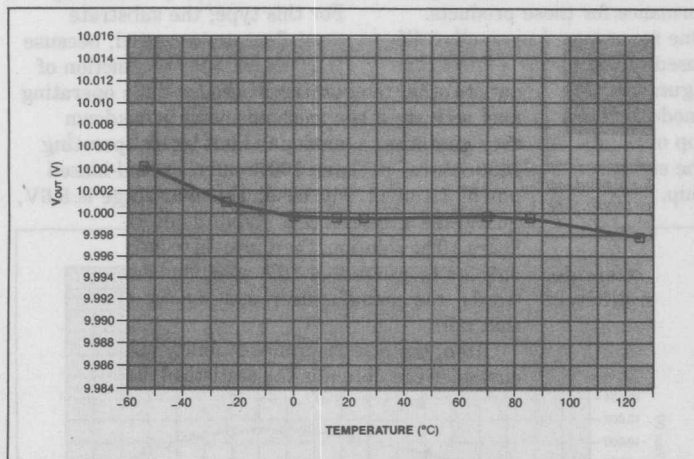


Fig D—The output of a diffused-zener reference such as the AD2710 provides excellent TC linearity from 0 to 70° C, but suffers in linearity outside that range.

Often, the statistical data taken by the manufacturer on life-test samples is the best stability information you can obtain about a reference.

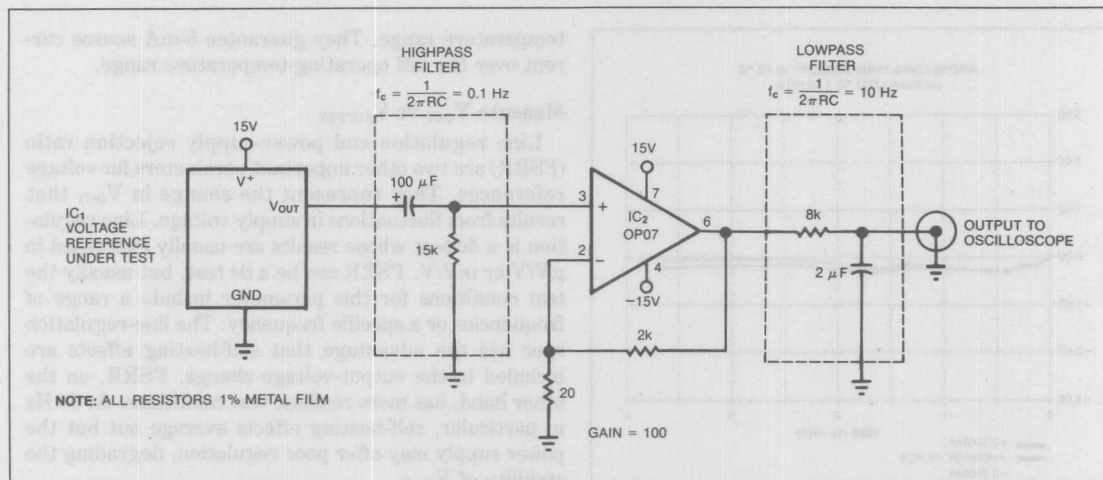


Fig 7—Introducing highpass and lowpass filters and a low-noise op amp lets you measure voltage-reference noise using a storage oscilloscope.

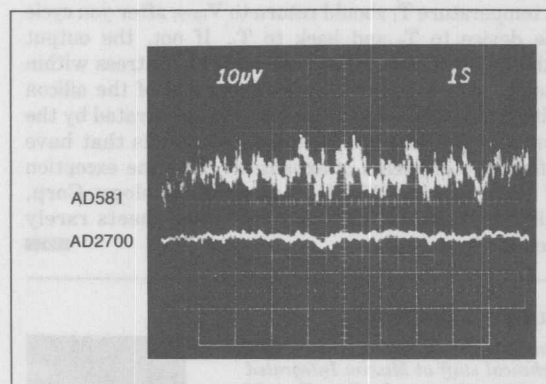


Fig 8—This scope photo shows the noise levels typical for a bandgap reference (upper trace) and a zener-based reference (lower trace). The scale is 10 μV/vertical div; 1 sec/horizontal div.

and about 5 μV p-p for the AD2700 zener reference. Table 1 compares noise for these devices over different bandwidths.

Long-term stability

Long-term stability can be the most important spec in a reference application, but—as in the case of noise—this parameter seldom receives a thorough characterization in the data sheet. Most manufacturers specify stability as 25 to 100 ppm (typ) per thousand hours at 125°C. They cannot accurately extrapolate this stability

TABLE 1—REFERENCE-NOISE COMPARISON

BANDWIDTH	NOISE (μV p-p)	
	AD581 (BANDGAP)	AD2700 (ZENER)
0.1 TO 10 Hz	20	5
1 TO 100 Hz	50	8
1 Hz TO 3 kHz	220	30
1 Hz TO 300 kHz	600	200

data to other temperatures because those temperatures may activate other mechanisms of instability. Nor can they guarantee a maximum limit by testing all parts for 1000 hours, because 100% burn-in testing costs too much. (And in any case, the manufacturer cannot guarantee a reference's stability for the second 1000 hours.) The solution, therefore, is to either test samples only or to guarantee this spec "by design" (in other words, the manufacturer will replace customer parts that fail).

Often, the best reference-stability information that a customer can obtain is the statistical data taken by the manufacturer on life-test samples. Maxim, for example, records long-term stability for a set of sample devices operating continuously for several thousand hours at 55°C (a realistic operating temperature that is higher than the room ambient temperature but lower than T_{MAX}). Such data (Fig 9) for the AD2700, for instance,

Output-current specs are misleading unless they specify V_{OUT} limits such as those in the spec for load regulation.

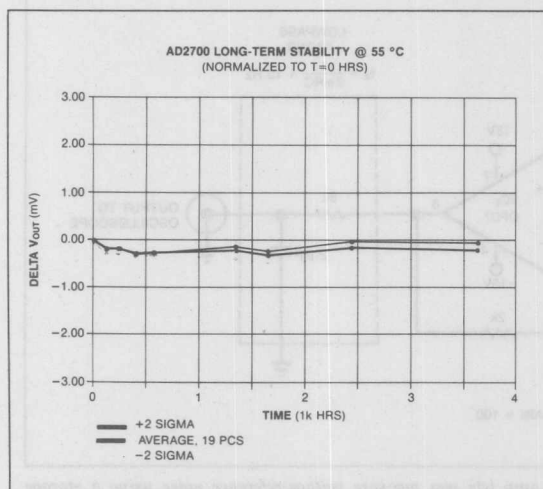


Fig 9—The average stability of AD2700 voltage references over 3600 hours at 55°C appears in the center curve. The upper and lower curves denote 2-sigma boundaries that encompass 90% of the 19 units tested.

shows that V_{OUT} drifts about 250 μV negative and then remains within $\pm 50 \mu V$ of that level. The center curve represents typical performance; the upper and lower "2-sigma" curves encompass 90% of the devices, based on the standard deviation of measured values.

I_{OUT} specs can be misleading

Output-current specs are misleading unless they specify V_{OUT} limits such as those included in the spec for load regulation. Note how this parameter reveals important differences in several reference devices. The AD2700, for example, has a 741-type output circuit that can sink and source current equally well within a range of ± 10 mA. V_{OUT} changes 0.5 mV max for a 0- to 10-mA change in output current, resulting in a load regulation of 50 μV /mA max.

The MAX671 has Kelvin outputs that provide load regulation of 10 μV /mA max. The 10V REF01 monolithic reference, on the other hand, has a simple emitter-follower output that can only source current (to ground); its load regulation is 1 mV/mA max over 0 to 10 mA. For the AD580, this same 1-mV/mA limit represents lower performance because V_{OUT} is only 2.5V. The 10V references AD581 and AD584 can source as much as 10 mA at 25°C but specify the load regulation (500 μV /mA max) to only 5 mA. These two devices have limited current-sinking capability over the MIL

temperature range. They guarantee 5-mA source current over the full operating-temperature range.

Measure V_{OUT} vs V_{SUPPLY}

Line regulation and power-supply rejection ratio (PSRR) are two other important parameters for voltage references. They represent the change in V_{OUT} that results from fluctuations in supply voltage. Line regulation is a dc test whose results are usually expressed in $\mu V/V$ or mV/V. PSRR can be a dc test, but usually the test conditions for this parameter include a range of frequencies or a specific frequency. The line-regulation spec has the advantage that self-heating effects are included in the output-voltage change. PSRR, on the other hand, has more realistic test conditions. At 60 Hz in particular, self-heating effects average out but the power supply may offer poor regulation, degrading the stability of V_{OUT} .

Finally, consider the implications of temperature hysteresis in your application. A reference output V_{OUT1} at temperature T_1 should return to V_{OUT1} after you cycle the device to T_2 and back to T_1 . If not, the output exhibits hysteresis. The cause is thermal stress within the IC, which in turn causes expansion of the silicon with temperature—and this effect is aggravated by the contact of dissimilar packaging materials that have different coefficients of expansion. With the exception of that for the LT1021 (Linear Technology Corp, Milpitas, CA), voltage-reference data sheets rarely mention hysteresis.

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Author's biography

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Back-to-basics approach yields stable references

Achieving the accuracy and stability that IC voltage references promise isn't necessarily a "piece of cake," but if you return to your EE roots and do a little old-fashioned analog-circuit analysis, you can obtain impressive results.

Ron Knapp, Maxim Integrated Products

Analog-IC manufacturers make it look simple to achieve the voltage-reference accuracy and stability that used to present major challenges for circuit designers. Today, obtaining stability of a few parts per million per degree should be a routine task. Nonetheless, ignoring facts of life such as noise and I-R drops can transform a seemingly simple job into one as complex as that faced by reference designers 20 years ago. Attention to circuit basics can make obtaining precise rock-solid reference voltages in the late 1980s as uncomplicated as the vendors of the ICs intend it to be.

Selecting a low-temperature-coefficient, precision voltage reference starts with careful consideration of your noise requirements. If the reference is too noisy, the highest dc accuracy and the cheapest price won't mean anything. Determine the signal-to-noise ratio your application requires. If you intend to use the

reference with an A/D or D/A converter, the reference noise should be less than $\frac{1}{10}$ the resolution. For example, a 12-bit ADC with a 0 to 10V input has a 1-LSB resolution of 2.44 mV. The maximum noise from the reference should be no more than 240 μ V p-p. In this case, a bandgap reference such as an REF01 or AD581 will suffice. For a 14-bit converter with an LSB size of 610 μ V, a noise limitation of 60 μ V will require an AD2700, MAX670, or equivalent.

Often, you can lower the wideband noise with a large capacitor placed on the reference-device output. A 10- μ F capacitor is large enough to prevent oscillation problems and will typically decrease the high-frequency noise (above 1 kHz) by a factor of 3 or 4. Some references, like the AD584, have noise-reduction pins that allow you to add an external capacitor. A smaller capacitor (0.01 μ F) placed in parallel with the feedback resistor (if the inverting input of the reference amplifier is available) will filter the noise from both the reference device and the amplifier, but will also adversely affect the turn-on time and the circuit's response to load changes. Nevertheless, there is little you can do about low-frequency noise, and therefore most reference data sheets place great importance on noise in the 0.1- to 10-Hz band.

Thermal effects take second place

Taking into account noise considerations, the second most important spec of a voltage reference is the temperature coefficient, or TC. Don't ignore initial

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Ignoring facts of life like noise and I-R drops can turn what appears to be a simple job into a complex one.

accuracy, though, or take it too lightly, thinking that you'll be able to adjust it. Remember that any components you add can jeopardize the TC, long-term stability, and reliability—all it takes is one component that drifts out of calibration. For example, using a reference's trim-adjust feature or scaling its output with an external gain stage will probably affect the TC.

To set the gain of an op amp, you should use TC-matched thin-film resistor networks. When you use separate RN55D metal-film resistors with TC specs of ± 50 ppm/ $^{\circ}\text{C}$, you introduce a TC error of 100 ppm/ $^{\circ}\text{C}$ if one resistor TC is $+50$ ppm/ $^{\circ}\text{C}$ and the other is -50 ppm/ $^{\circ}\text{C}$. The fine-trim adjustment of the AD2700 is somewhat interactive with the TC; 1 mV of adjustment changes the TC by $4 \mu\text{V}/^{\circ}\text{C}$ or 0.64 ppm/ $^{\circ}\text{C}$ referred to the output. The best advice to follow about reference trim adjustment is "don't do it." It is much better to calibrate the gain elsewhere—at the D/A converter, for example. Better yet, make gain adjustments in software. If there is a temperature-independent gain trim elsewhere in the system, you can use the AD2700's fine-trim output-voltage adjustment to change the device's TC (and, incidentally, affect its output voltage).

High-resolution converters need TLC

Most high-resolution converters, such as 16-bit DACs and ADCs, guarantee linearity consistent with resolution, but rarely do they guarantee absolute accuracy, which includes gain error, to that level. Because the gain accuracy depends primarily on the accuracy of the voltage reference (whether internal or external), the temperature coefficient of the reference determines the useful temperature range for converter accuracy (Fig 1). Applications where absolute accuracy is critical include weighing scales, data-acquisition measurement systems, automatic test equipment (ATE), and laboratory instruments (such as DVMs and programmable voltage standards).

First, consider a 12-bit-system example. A 12-bit A/D converter with its linearity specified to $\pm \frac{1}{2}$ LSB requires a reference with a TC of no more than 2.67 ppm/ $^{\circ}\text{C}$ from 25 to 70°C to maintain a gain accuracy within $\frac{1}{2}$ LSB, or 1.2 mV out of 10V FS. A suitable reference would be the AD2710KD, which is specified to 2 ppm/ $^{\circ}\text{C}$ max from 0 to 70°C .

For a 16-bit system, you can use a reference guaranteed to 1 ppm/ $^{\circ}\text{C}$, like a MAX671 or an AD2710LD, to obtain true 16-bit absolute accuracy over the 7.5°C range from 25 to 32.5°C . Between these temperatures, the output of the reference changes no more than 75

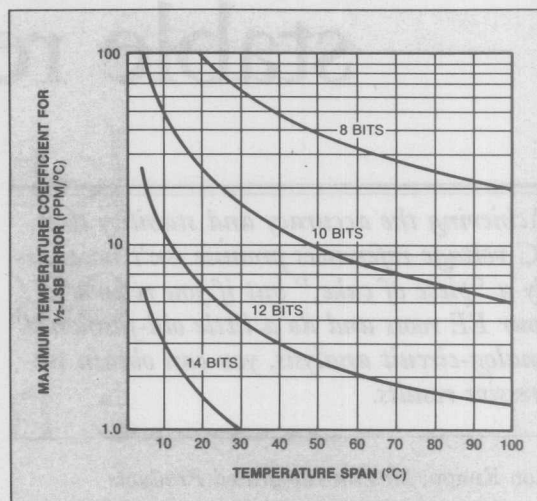


Fig 1—Increasing the resolution of an A/D or D/A converter decreases the temperature range over which it delivers absolute accuracy comparable to its resolution.

μV —an amount equivalent to less than $\frac{1}{2}$ LSB on a 16-bit, 10V FS converter.

Most voltage references on the market produce a single-ended output between V_{OUT} and GND, as in the AD2700, REF01, AD580, AD581, and AD584. In these types of devices, I-R voltage drops can cause errors that can spoil the accuracy of the output voltage. The reason is that the load current must pass through the V_{OUT} pin and the quiescent supply current must pass through the GND pin (Fig 2). If the output happens to be sinking current—for example, if the load is connected between V_{OUT} and V^+ as in Fig 3—then the load current also returns through the GND pin. In most cases, however, the load is connected between V_{OUT} and GND; the load current flows into the reference from V^+ and out to the load through the V_{OUT} pin. In these cases, the I-R drop on GND won't disturb the output voltage, but the I-R drop on the V_{OUT} pin will always remain.

You can minimize single-ended output errors by using a device whose package incorporates internal Kelvin connections (that is, separate force and sense lines) to connect the die to the package pins (Fig 2). Running both force and sense bond wires internally from the chip to the output pin places the "force" bonding wire's resistance inside the output amplifier's feedback loop. This technique in effect eliminates connection resistance except for that of the pin itself and

that of the wiring or metal trace between the output and the load. With many references operating at full output current, even if you connect the load directly to the pin, the voltage drop in the pin resistance itself is large enough to equal the initial accuracy spec.

Small errors add up

For example, the AD2710LD has an initial accuracy of $10.000\text{V} \pm 1\text{ mV}$ max. The device is enclosed in a 14-lead ceramic sidebraced DIP that can have a pin resistance of 0.05Ω (Fig 2). If your circuit draws the full output current of 10 mA , the resulting voltage drop in series with the load will be 0.5 mV —half the initial accuracy spec. This drop has the effect of lowering the output voltage to 9.9995V (assuming that the factory set it to exactly 10.0000V with no load).

If you connect the load to V^+ as in Fig 3, the error will be twice as great, because the GND I-R drop is additive. The result is a further decrease in load voltage, to 9.9990V . In fact, the output-lead resistance is the dominant contribution to the load-regulation spec of $50\text{ }\mu\text{V}/\text{mA}$, which is equivalent to 0.05Ω . The I-R-induced errors can expand into several millivolts if there is any length of wiring or pc-board trace that measures a few tenths of an ohm.

For constant-current loads, it's possible to simply

adjust out the errors caused by I-R drops. However, the TC of the reference may be unacceptable because the TC of the pin resistance is too high. Gold has a TC of $4000\text{ ppm}/^\circ\text{C}$, or $0.4\%/^\circ\text{C}$. With this TC, the 0.05Ω resistance in the above example would increase by 40% between 25 and 100°C . At 100°C , the resistance is 0.07Ω and produces a 0.7-mV error at a load current of 10 mA .

Sense at the load

A voltage reference can easily eliminate all the problems associated with I-R drops if it uses Kelvin outputs with separate force and sense pins joined at the load. The sense pin carries only a small, constant current, such as that which flows in the gain-determining feedback resistors. The force pin carries all of the variable load-dependent current. You close the feedback loop at the load by connecting the force and sense pins there; that is, you place the wiring and pin resistances inside the feedback loop.

Because of limitations on the number of package pins, some references provide only one GND pin and offer Kelvin connections only on the output. This setup is adequate if the output sources current but does not sink it, as is true in the majority of applications. The MAX670 and MAX671 contain full Kelvin connections

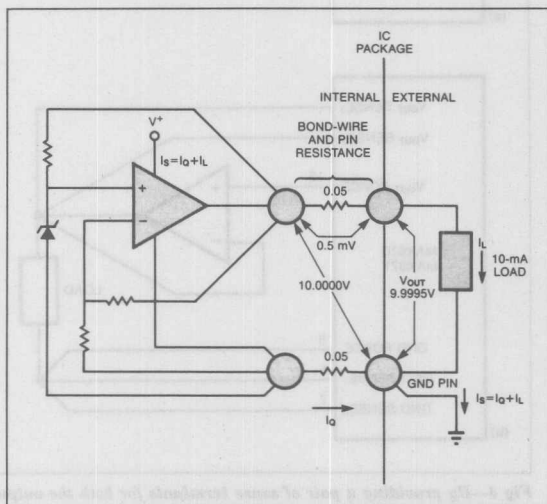


Fig 2—When this reference supplies current to a load, voltage drops inside the package are inside the feedback loop and have little effect on accuracy. The voltage drop across the package's output pin can be significant, however.

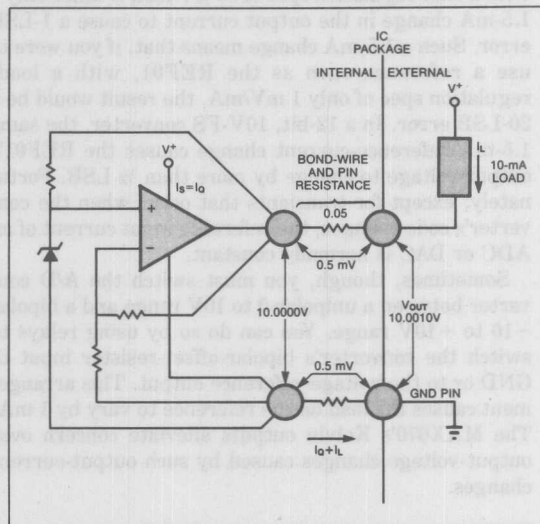


Fig 3—If a reference sinks current into its output from the positive supply, both the voltage drop across the package's ground pin and the drop across its output pin will affect accuracy.

Don't take the initial accuracy too lightly, thinking that you'll be able to adjust it.

on both output and GND (Fig 4a). These devices can source or sink 10 mA.

Why are Kelvin output connections so important? First of all, they make the voltage reference easier to use: You can preserve accuracy without providing extra-wide printed-circuit traces or limiting the load current or the length of the wire that carries it. (You do, however, need to consider the possibility of loop instability caused by the inductance of the load-current-carrying wires and capacitive loading of the feedback network.)

Fifty milliohms can be a big deal

D/A and A/D converters with 12- to 16-bit resolution often require separate voltage references. In the case of a 16-bit converter, if the full-scale input equals 5V, 1 LSB has a value of 76.25 μ V. As good as the AD2700 is, with a load-regulation spec of 50 μ V/mA, it takes only a 1.5-mA change in the output current to cause a 1-LSB error. Such a 1.5-mA change means that, if you were to use a reference such as the REF01, with a load-regulation spec of only 1 mV/mA, the result would be a 20-LSB error. In a 12-bit, 10V-FS converter, the same 1.5-mA reference-current change causes the REF01's output voltage to change by more than $\frac{1}{2}$ LSB. Fortunately, except for transients that occur when the converter's code changes, the reference input current of an ADC or DAC is normally constant.

Sometimes, though, you must switch the A/D converter between a unipolar 0 to 10V range and a bipolar -10 to +10V range. You can do so by using relays to switch the converter's bipolar-offset-resistor input to GND or to the voltage-reference output. This arrangement causes the load on the reference to vary by 1 mA. The MAX670's Kelvin outputs alleviate concern over output-voltage changes caused by such output-current changes.

Buffering—analgesic for pain of high current

The MAX670 and the MAX671 are unusual in the way that their Kelvin sense lines are further divided between two separate pins (Fig 4a). This arrangement allows you to add an output buffer transistor or amplifier for higher current. It also allows you to place the added components within the reference feedback loop and thus maintain the specified performance at the load (Fig 4b). For example, an LH0101, together with a MAX670, can supply 10V at 2A with a 3-ppm/ $^{\circ}$ C TC. In this way, the MAX670 can serve as an ultrastable, low-noise power-supply regulator with an output cur-

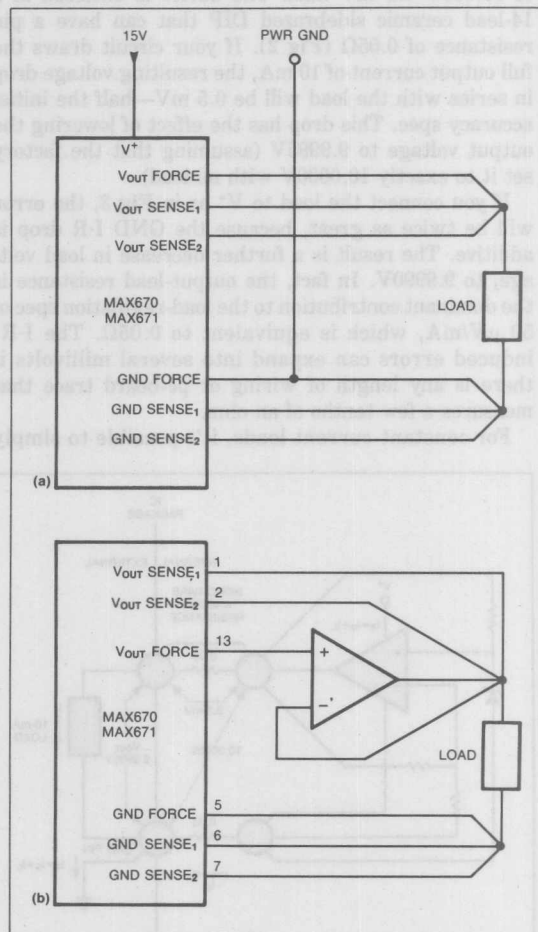


Fig 4—By providing a pair of sense terminals for both the output and ground signals (a), this reference can compensate for voltage drops outside as well as inside the package (b). The configuration also allows you to enclose a high-current output buffer within the feedback loop.

rent ranging from hundreds of milliamps to a few amps, depending on the external buffer components.

You can use an amplifier to buffer references without Kelvin connections, but the voltage at the load is subject to added errors such as offset, drift over temperature, output-impedance-induced voltage drops, and voltage variations caused by line regulation. If you know the load current to within ~20%, you can supply high current regardless of the type of reference, even if

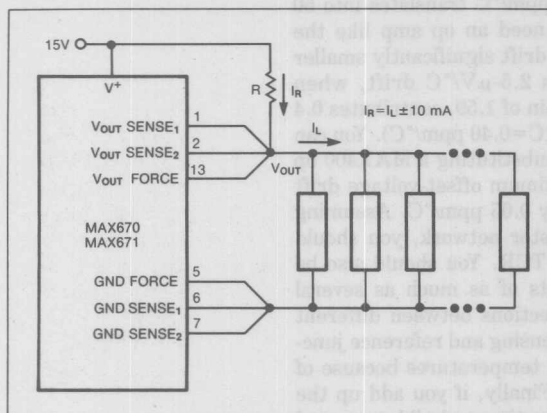


Fig 5—A pullup resistor acts as a poor man's output buffer by delivering most of the load current. Even though it delivers a small fraction of the load current, the reference still controls the output voltage.

it is one with a single-ended output (Fig 5). In such a special case, you can use a pullup resistor to supply the nominal load current from V^+ to V_{OUT} . The reference output then only needs to sink or source the error current—the difference between the actual load current and that supplied by the resistor. Most IC-op-amp outputs supply at least ± 10 mA. Ideally, if the pullup current exactly equals the load current to ground, the output current from the voltage reference will be zero. When using references like the REF01, which can source current but cannot sink it, you must guarantee that the current in the pullup resistor is less than the load current, so that the reference always supplies some current. The REF01 supplies 10 mA to ground, so you should select the pullup resistor to supply 5 mA less than the load current. That way, the REF01 will nominally supply 5 mA, a value in the middle of its range.

This technique is prevalent in ATE, where one reference supplies the reference input to perhaps dozens of D/A converters, which set the voltage or current of the pin drivers that supply signals to the device under test. A similar situation arises in drift testing large numbers of D/A converters in a temperature chamber; a reference outside the chamber drives the reference input of all of the converters.

All in all, there are three advantages to using a pullup resistor to boost a reference's output-drive capability: Adding a single passive component is simple and cheap; you preserve the accuracy and TC performance

of the reference without resorting to Kelvin connections; and you don't need extra supply current (as you would if you used a buffer).

Why not design your own?

Voltage references seem like simple circuits, so you might be tempted to design your own with discrete components, but you should consider the tradeoffs carefully. To make a bandgap reference like the REF01, for instance, you need two transistors carrying equal currents with an 8:1 current-density ratio. In other words, one transistor must have 8 $\times$ the emitter area of the other. Matched pairs that have this area ratio are not commonly available, but you could use a pair of identical devices and set the current ratio with resistors, except that the TC of the resistors must match as do the TCs of R_1 and R_2 in Fig 6. In addition, you still have to amplify the 1.2V bandgap voltage, something that requires an op amp with matching gain resistors (R_5 and R_6 in Fig 6).

If you want to construct a reference similar to the AD2700 (Fig 2), you can do so with a 1N829 5-ppm/ $^{\circ}$ C zener diode and an op amp, but again don't forget the task's nontrivial nature. First of all, the diode's several-dollar price tag is a significant expense. And, in discrete form, the best temperature-compensated diodes have TC specs higher than the AD2700 spec. Assuming you can accept 5 ppm/ $^{\circ}$ C, however, you'll need a low-

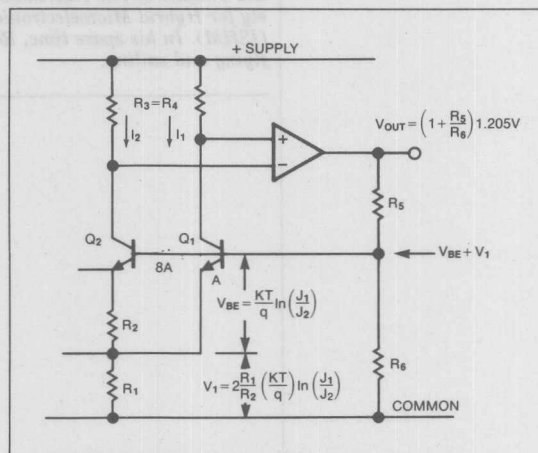


Fig 6—A bandgap voltage reference generates the sum, $V_{BE} + V_1$, in which the two voltages have equal and opposite temperature coefficients. The amplifier then raises the sum to a more convenient voltage level.

drift op amp. The spec of 5 ppm/°C translates into 50 $\mu\text{V}/^\circ\text{C}$, and therefore you'll need an op amp like the OP07, with an offset voltage drift significantly smaller than 50 $\mu\text{V}/^\circ\text{C}$. The OP07's 2.5- $\mu\text{V}/^\circ\text{C}$ drift, when multiplied by the required gain of 1.59, contributes 0.4 ppm/°C (10V/6.3V-0.25 ppm/°C=0.40 ppm/°C). You can reduce this drift further by substituting a MAX400 op amp: It has a 0.3- $\mu\text{V}/^\circ\text{C}$ maximum offset-voltage drift spec, which translates to only 0.05 ppm/°C. Assuming that you use a thin-film resistor network, you should allow a 0.5-ppm/°C tracking TCR. You should also be aware of thermocouple effects of as much as several $\mu\text{V}/^\circ\text{C}$, a result of interconnections between different metals. The thermocouples' sensing and reference junctions are at slightly different temperatures because of gradients across the board. Finally, if you add up the cost of the components and the time to build, test, and calibrate the circuit, you can easily appreciate the value of purchasing a complete, tested, and guaranteed precision voltage reference. **EDN**

Author's biography

Ron Knapp is a senior member of the technical staff at Maxim Integrated Products (Sunnyvale, CA). He holds a BS in systems engineering from Boston University and an MSEE from Worcester Polytechnic Institute. He is vice president of the Northern California Chapter of The International Society for Hybrid Microelectronics (ISHM). In his spare time, Ron enjoys flying and sailing.



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Ultra-Low Current Shunt Amplifier

This circuit measures the power supply current of a circuit without really requiring a current shunt resistor: R1 is only 3 centimeters of #20 gauge (0.8mm diameter) copper wire. A length of the power distribution wiring can be used for R1. The MAX420's CMVR includes its own negative power supply, therefore it can both be powered by, and measure current in, the ground line.

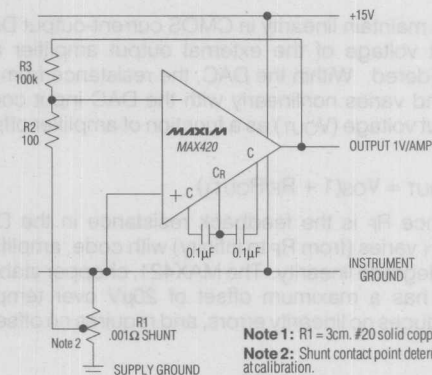


Figure 5-1.

One Op-Amp Thermocouple Amplifier

The MAX420 is operated at a gain of 191 to convert the $52\mu\text{V}/^\circ\text{C}$ output of the type J thermocouple to a $10\text{mV}/^\circ\text{C}$ signal. The $-2.2\text{mV}/^\circ\text{C}$ tempco of the 2N3904 is added into the summing junction with a gain of 42.2 to provide cold junction compensation. The ICL8069 is used to remove the offset caused by the 600mV initial voltage of the

2N3904. Adjust the 10K trimpot for the proper reading with the 2N3904 and isothermal connection block at a temperature near the center of the circuit's operating range. Use the component values shown in parentheses when using a type K thermocouple.

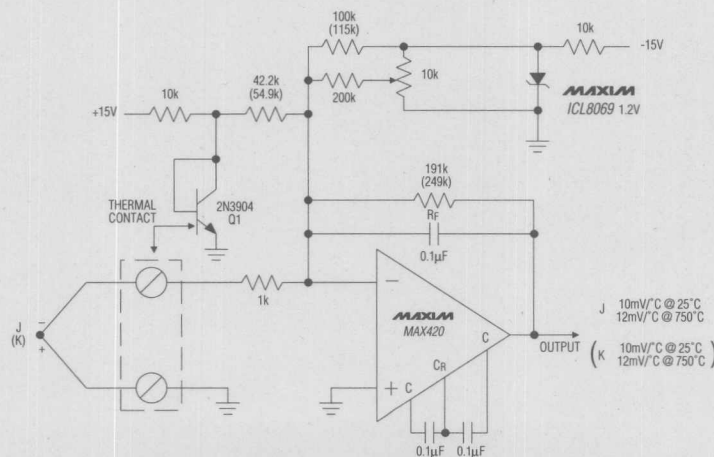


Figure 5-2.

To maintain linearity in CMOS current-output DACs, the offset voltage of the external output amplifier must be considered. Within the DAC, the resistance from IOUT1 to ground varies nonlinearly with the DAC input code. The output voltage (VOUT) as a function of amplifier offset (VOS) is:

$$V_{OUT} = V_{OS}(1 + R_F/R_{OUT1})$$

Since R_F is the feedback resistance in the DAC and R_{OUT1} varies (from R_F to infinity) with code, amplifier offset can degrade linearity. The MAX421, chopper stabilized op amp has a maximum offset of 20µV over temperature, introduces no linearity errors, and requires no offset adjustment.

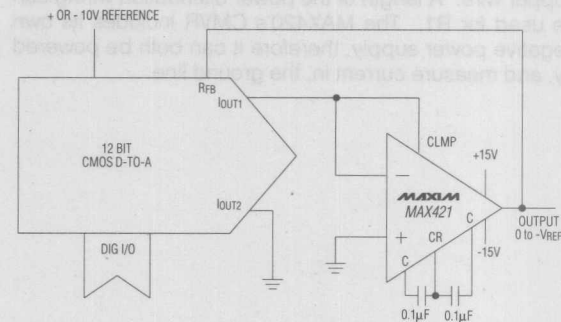


Figure 5-3. Low offset maintains DAC linearity.

Strain Gauge Instrumentation Amplifier

This circuit has an overall gain of 330. More gain can easily be obtained by lowering the value of R2. Untrimmed V_{OS} is $10\mu V$, and V_{OS} tempco is less than $0.1\mu V/^{\circ}C$. In

many circuits, the MAX400 can be omitted, with the two MAX421 differential outputs connected directly to the differential inputs of an integrating A/D.

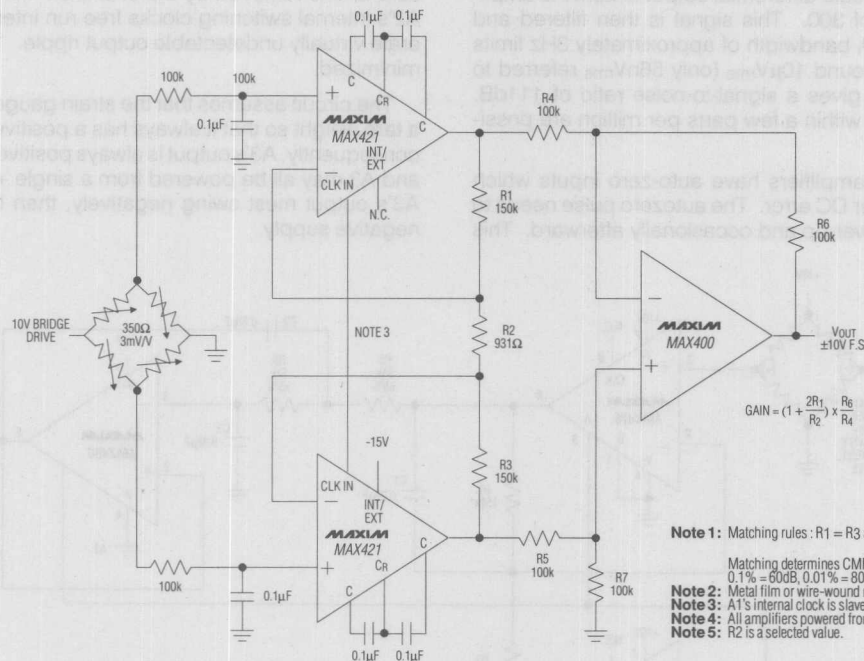


Figure 5-4. $10\mu V$ V_{OS} , $0.1\mu V/^{\circ}C$ Strain Gauge Instrumentation Amplifier

Low Drift High Speed Power Op Amp

This circuit has the DC V_{OS} and gain characteristics of the MAX420, and the power handling and high speed AC characteristics of the LH0101.

The MAX420 monitors and integrates the offset error at the inverting input of the LH0101, then adjusts the non-inverting input such that the inverting input voltage is within $5\mu V$ of ground. The $10k/47\Omega$ attenuator between the MAX420 and the LH0101 input scales the offset adjustment range such that a $\pm 10V$ swing at the MAX420 output corrects for $\pm 50mV$ of offset in the LH0101.

The MAX420 does not compensate for the output voltage error of the LH0101 $I_{BIAS} \times R_{FDBK}$, but this can be made negligible in most systems since the LH0101 I_{BIAS} is only $1nA$.

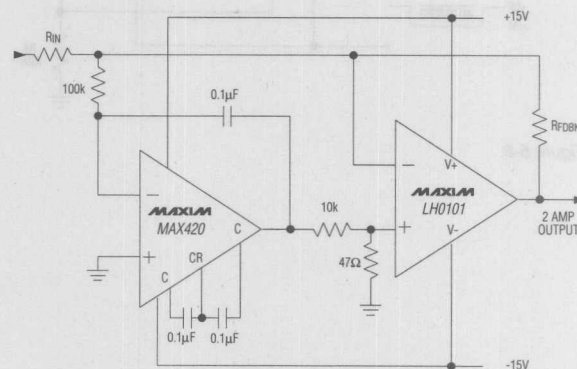


Figure 5-5.

This amplifier connection uses two MAX426 precision amplifiers (A1 and A2), with appropriate gain resistors (R1 through R4) to amplify the output of a strain gauge bridge. The bridge's full-scale differential output of 20mV is amplified by a factor of 300. This signal is then filtered and buffered by A3. A bandwidth of approximately 3Hz limits output noise to around $10\mu\text{V}_{\text{rms}}$ (only 56nV_{rms} referred to the input), which gives a signal-to-noise ratio of 111dB. Measurements to within a few parts per million are possible.

The two input amplifiers have auto-zero inputs which correct all amplifier DC error. The autozero pulse needs to be applied on power-up and occasionally afterward. This

pulse may be applied as infrequently as every 30 minutes or more because the effect of amplifier drift appears only as a small 300Hz ripple signal with an average value of zero and is removed by the 3Hz filter. Amplifiers A1 and A2's internal switching clocks free run internally, but generate virtually undetectable output ripple. 1/f noise is also minimized.

The circuit assumes that the strain gauge is loaded with a tare weight so that it always has a positive output signal. consequently, A3's output is always positive so that A1, A2, and A3 may all be powered from a single +10V supply. If A3's output must swing negatively, then it will require a negative supply.

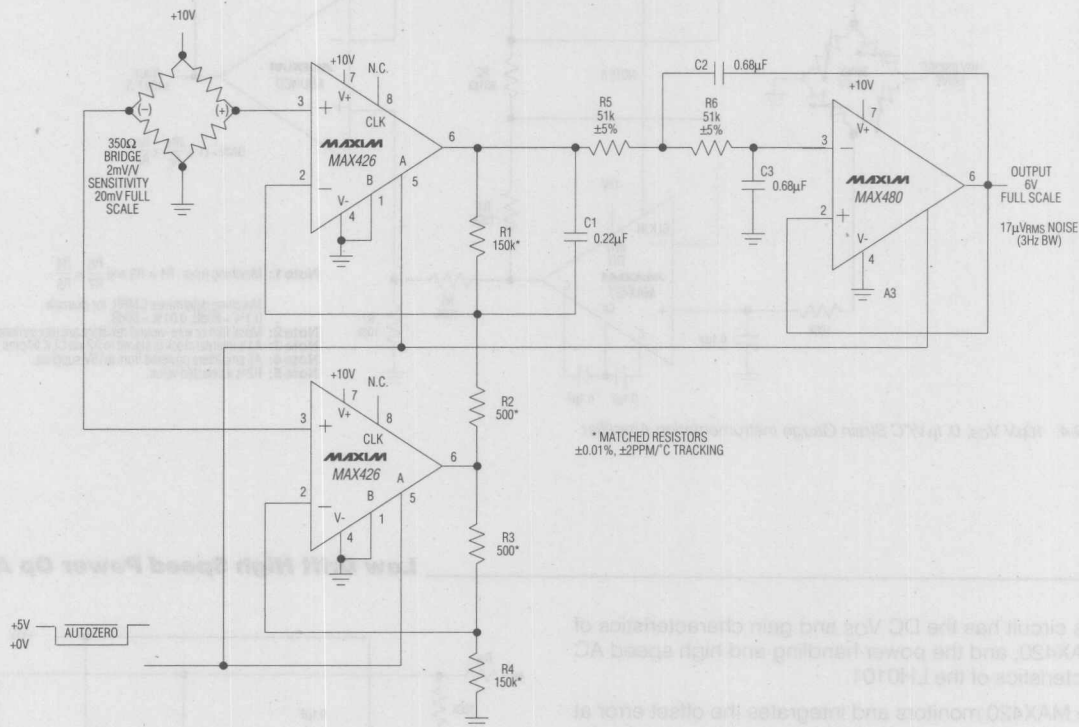


Figure 5-6.

Two MAX455s can be cascaded to form a 1 of 15 video mux by connecting the output of one mux to one of the input channels of a second mux. Although the two devices

are usually close to one another, the output of the first mux should be terminated to preserve its bandwidth.

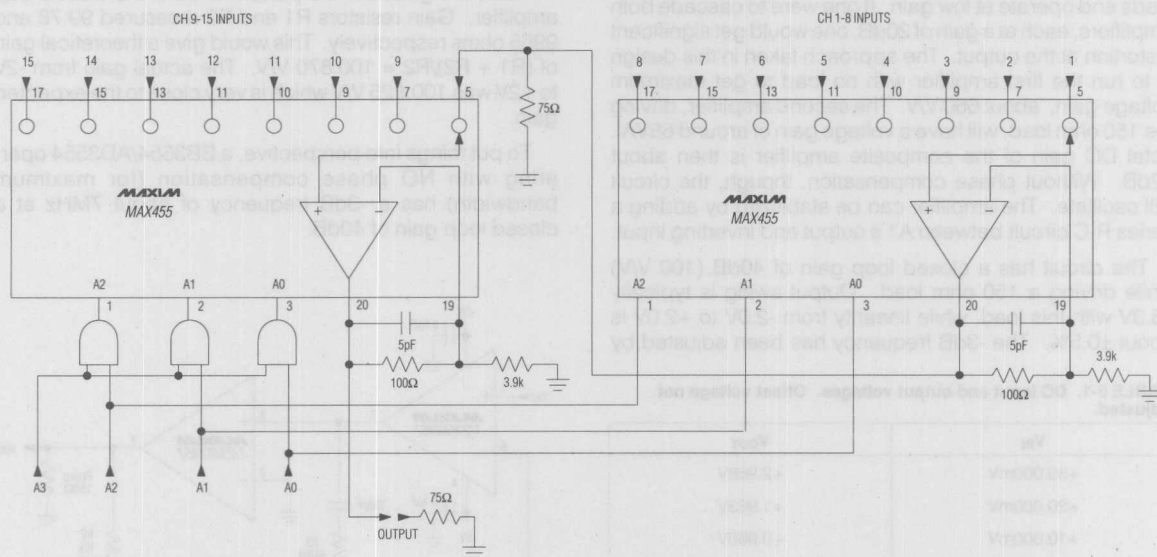


Figure 5-7.

2 Channel Lossless Video Switch

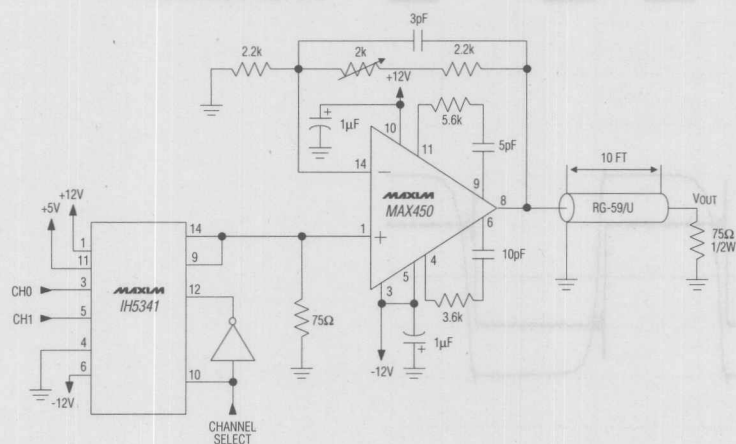


Figure 5-8.

By cascading both amplifiers of a MAX457 (dual video amplifier) and adding appropriate phase compensation, one can build a composite amplifier that has high gain and wide bandwidth while exhibiting good DC accuracy. These video amplifiers normally drive either 75 or 150 ohm loads and operate at low gain. If one were to cascade both amplifiers, each at a gain of 20dB, one would get significant distortion at the output. The approach taken in this design is to run the first amplifier with no load to get maximum voltage gain, about 660 V/V. The second amplifier, driving the 150 ohm load, will have a voltage gain of around 65V/V. Total DC gain of the composite amplifier is then about 92dB. Without phase compensation, though, the circuit will oscillate. The amplifier can be stabilized by adding a series R-C circuit between A1's output and inverting input.

The circuit has a closed loop gain of 40dB (100 V/V) while driving a 150 ohm load. Output swing is typically $\pm 3.3\text{V}$ with this load, while linearity from -2.0V to +2.0V is about $\pm 0.5\%$. The -3dB frequency has been adjusted by

R and C to be 10MHz (gain x bandwidth = 1GHz). A frequency sweep shows only about 3% peaking near the roll-off frequency. Full output swing of $\pm 2\text{V}$ is achieved over the 10MHz bandwidth.

Table 5-1 gives the DC performance of the closed loop amplifier. Gain resistors R1 and R2 measured 99.78 and 9965 ohms respectively. This would give a theoretical gain of $(R1 + R2)/R2 = 100.870 \text{ V/V}$. The actual gain from -2V to +2V was 100.825 V/V which is very close to the expected gain.

To put things into perspective, a BB3554/AD3554 operating with NO phase compensation (for maximum bandwidth) has a -3dB frequency of about 7MHz at a closed loop gain of 40dB.

TABLE 5-1. DC input and output voltages. Offset voltage not adjusted.

V _{IN}	V _{OUT}
+30.000mV	+2.968V
+20.000mV	+1.963V
+10.000mV	+0.960V
0.000mV	-0.046V
-10.000mV	-1.060V
-20.000mV	-2.070V
-30.000mV	-3.059V

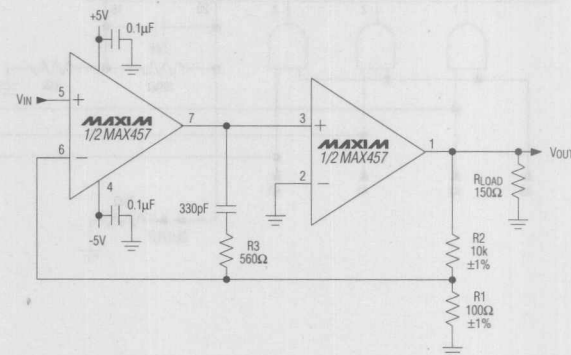


Figure 5-9. Schematic of composite amplifier with 40dB of gain and 10MHz bandwidth.

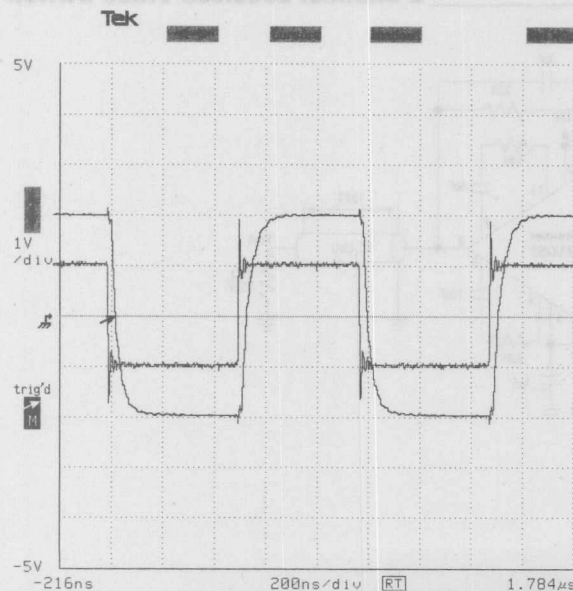


Figure 5-10.

Test boards often need to measure the magnitude of AC sine waves over a wide frequency range. The circuit shown here uses a dual video amplifier to make an average responding AC to DC converter. The MAX457 was selected because it has high input impedance, wide bandwidth, fast slew rate, and a transconductance output stage. (A transconductance output stage is desired when building active rectifier circuits).

The first amplifier, A1, is just a scaling amplifier. The amplifier's MOSFET input stage provides a high input impedance so that the signal source is not loaded appreciably by the amplifier. Closed loop gain of this first stage is set by R1 and R2. The signal needs boosting to make up for the small signal losses of the low (open loop) gain of the video amplifiers, and also to scale to output for an average equivalent RMS DC voltage. R3 and C3 are needed to make A1 unity gain stable.

The second amplifier, A2, is an active full-wave rectifier circuit with a differential DC output signal. R5, R6, and D1 rectify positive output signals; R7, R8, and D2 rectify negative output signals. R9, R10, C4, and C5 form two lowpass filters. The DC output consists of two signals (+DC, -DC), but one can use just a single output (e.g., +DC) and multiply by 2.

Table 5-2 gives the DC performance of the AC to DC converter. A Fluke 8920A True rms voltmeter was used to monitor the input to the circuit. Although the converter circuit is optimized for signals in the 0.1 to 1.0 Vrms range, it worked well down to 10 mVrms, reaching -3dB at 1MHz. For signals ranging from 100mV to 1.5Vrms, the converter gave useable response out to 10MHz. Because of the limited voltage swing of the video amplifiers, signal level is limited to 1.5Vrms sine waves.

TABLE 5-2. DC Output Voltage (+DC - (-DC)) in VDC vs. Frequency

V _{IN} (Vrms)	Frequency (MHz)								
	.001	.010	.100	1.00	2.00	3.00	5.00	7.00	10.0
0.010	.0096	.0096	.0094	.0072	.0045	—	—	—	—
0.030	.0298	.0298	.0296	.0279	.0238	.0205	.0142	.0076	—
0.100	.1002	.1002	.999	.968	.931	.894	.828	.752	.616
0.300	.3016	.3015	.3011	.2959	.2914	.2876	.2815	.2728	.2570
1.000	1.005	1.005	1.003	.995	.986	.979	.970	.948	.920
1.500	1.492	1.493	1.489	1.478	1.464	1.446	1.398	1.351	1.284

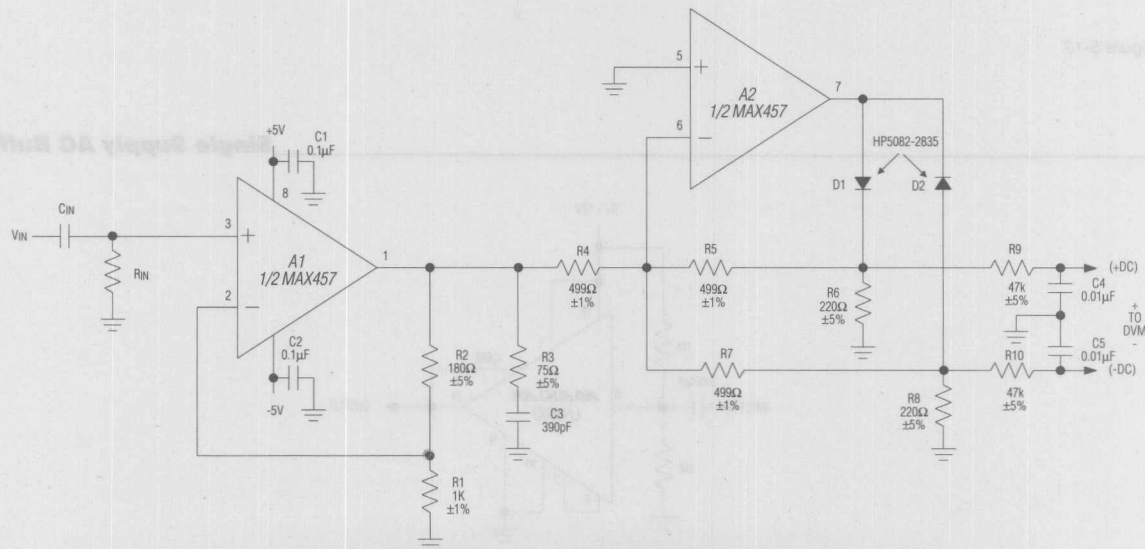


Figure 5-11. AC Sinewave to DC Converter (1Vrms in > 1VDC out)

Coaxial Cable Driver

With an input resistance of $10^{11}\Omega$ and input capacitance of 4pF, the LH0033 places negligible load on a 50 or 75 Ω video source. The Maxim LH0033A is guaranteed for operation with $\pm 5V$ power supplies common in video systems, and is also specified for a minimum $\pm 2V$ swing into a 75 Ω load. The LH0033 typically has only 2 degrees of phase non-linearity over the frequency range of 1 to 20MHz. The 68 Ω resistor on the output can be shorted out if a higher output voltage is required, but this causes a mitermination of the 75 Ω cable, and reflections will not be absorbed by the coaxial driver output.

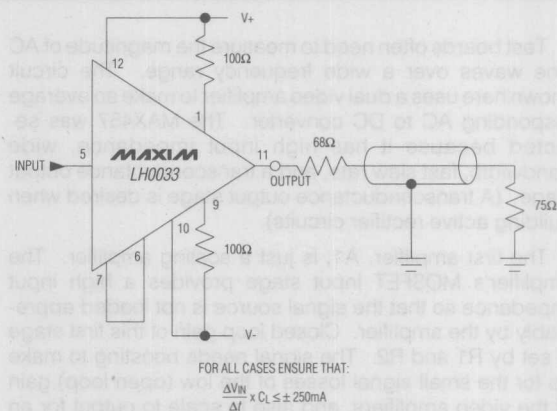


Figure 5-12. Coaxial Cable Driver

Instrumentation Shield/Line Driver

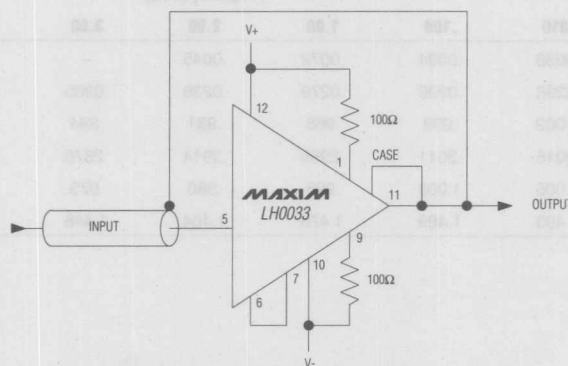


Figure 5-13.

Single Supply AC Buffer

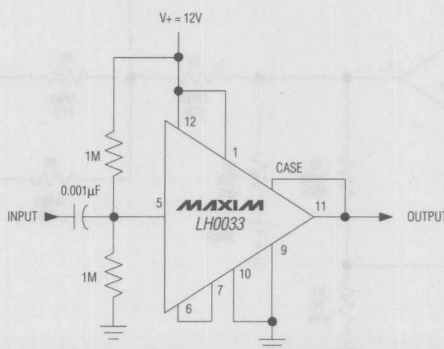


Figure 5-14.

Four LH0033A buffers form a video distribution amplifier capable of driving a number of 75Ω output lines from a single source with very low signal loss. The amplifiers operate from $\pm 5V$ supplies with a total power dissipation of 640mA plus the output power. Input resistance is negligible in most situations. The input capacitance, however, should be considered as it may result in high frequency misterminations at the input. Voltage gain is specified at typically 0.91, 0.84 min ($\pm 5V$ supplies and 75Ω load), so the worst case insertion loss of the distribution amplifier is 1.5dB, and is typically under 1dB. Protection resistors are included in series with pins 10 and 12 of each device so that the distribution amplifier tolerates momentary overloads on the outputs.

Figure 5-15 is a similar video distribution amplifier which has output resistance of 75Ω to back terminate the outputs. The back termination resistor is selected to be 68Ω to account for the typical 6Ω output resistance of the LH0033. Because each 75Ω load is isolated from the buffer amplifier, each device is able to drive two loads. The voltage loss through this amplifier will be approximately 6dB. Note that protection resistors are unnecessary in the back terminated configuration, as the LH0033 can safely drive the 68Ω termination resistor even if the cable is shorted.

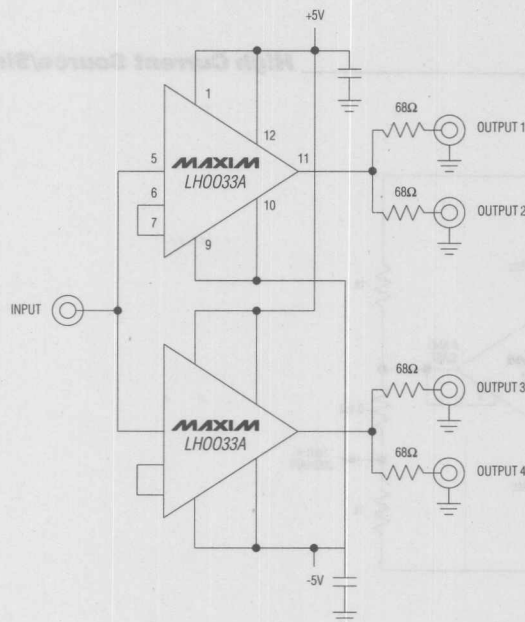


Figure 5-16.

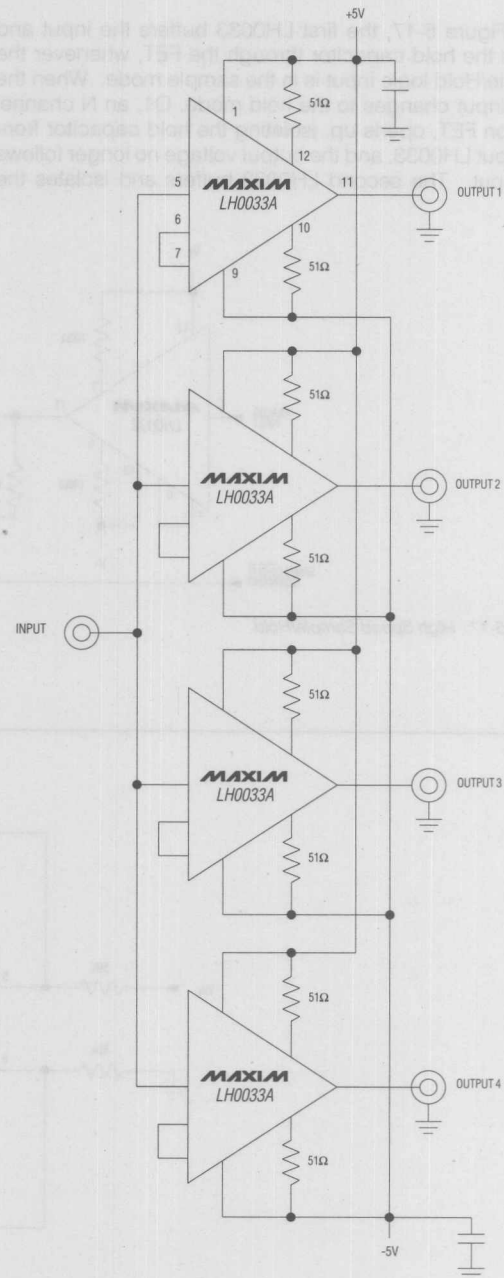


Figure 5-15.

In Figure 5-17, the first LH0033 buffers the input and drives the hold capacitor through the FET, whenever the Sample/Hold logic input is in the sample mode. When the logic input changes to the hold mode, Q1, an N channel junction FET, opens up, isolating the hold capacitor from the input LH0033, and the output voltage no longer follows the input. The second LH0033 buffers and isolates the

sample capacitor voltage from the load. Since the input bias current of the LH0033 is typically less than 1 nanoamp, the droop rate of this sample-and-hold is less than 1 mV/ms.

Since the LH0033 has a slew rate of 1500 V/ μ s and a 100MHz bandwidth, this LH0033-based sample-and-hold is well suited for use with video speed flash A/D converters.

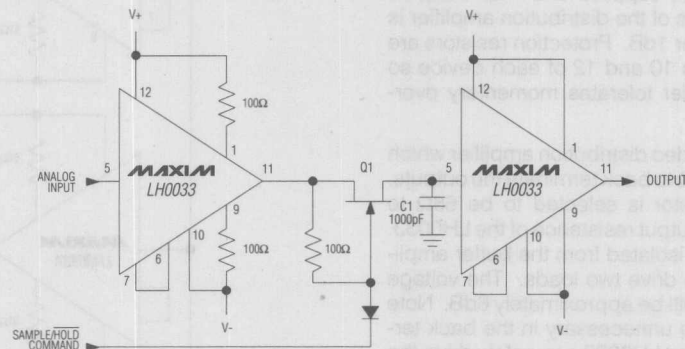


Figure 5-17. High Speed Sample/Hold

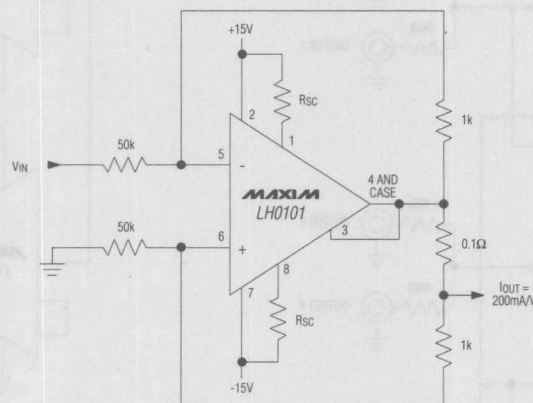


Figure 5-18. High Current Source/Sink

Figure 5-19 shows a voltage feedback DC servomotor amplifier. This type of control loop is normally used when the speed control is achieved by controlling the motor voltage. With the resistor values shown, the voltage at the motor will be $-5V_{IN}$. The output voltage is sensed at the motor, therefore voltage drops in the cable between the LH0101 and the motor will not affect the voltage applied to the motor. The 10Ω resistor and $0.01\mu F$ capacitor may be required to prevent oscillations.

Figure 5-20 shows a current feedback DC servomotor amplifier. This type of control loop is normally used to develop a torque approximately proportional to the input voltage. Like Figure 5-19, this circuit delivers a constant current that is proportional to the input voltage.

Figure 5-21 combines both current and voltage feedback to achieve better open loop speed regulation than can be achieved by either Figure 5-19 or 5-20. The specific values of R_S , R_{FI} and R_{GI} are chosen to best approximate the Speed/Current/Torque characteristic of the motor. Capacitor C_C may be required for stability if the positive feedback is such that the motor speed increases with increased torque load.

These circuits will either source or sink current, depending on the polarity of the input voltage, and can drive DC motors in both directions.

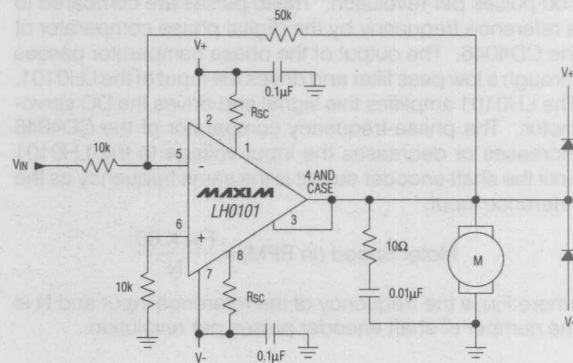


Figure 5-19. Servo Motor Amplifier.

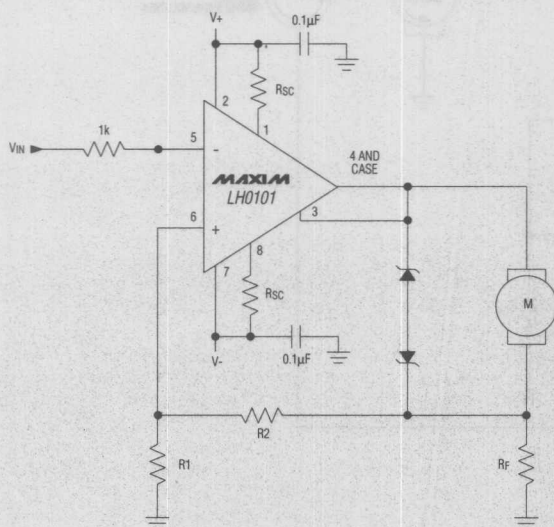


Figure 5-20. Torque Feedback Servo Motor Amplifier.

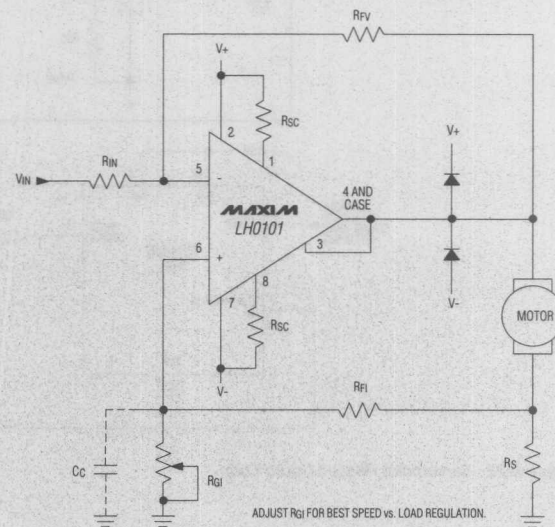


Figure 5-21. Constant Speed Motor Driver.

In the circuit of Figure 5-22, the shaft encoder produces 600 pulses per revolution. These pulses are compared to a reference frequency by the digital phase comparator of the CD4046. The output of the phase comparator passes through a low pass filter and drives the input of the LH0101. The LH0101 amplifies this signal and drives the DC servomotor. The phase-frequency comparator of the CD4046 increases or decreases the input voltage to the LH0101 until the shaft encoder output is the same frequency as the reference input.

$$\text{Motor Speed (in RPM)} = \frac{F_{IN} \times 60}{N}$$

where F_{IN} is the frequency of the reference input and N is the number of shaft encoder pulses per revolution.

A single-pulse-per-revolution speed pickup can be used in place of the shaft encoder, but the PLL low pass filter time constant must be greatly increased.

Note that this circuit is similar to a standard phase locked loop except that the LH0101, the motor, and the shaft encoder replace the internal VCO of the CD4046. Unlike the VCO of the CD4046, the motor adds another pole to the system response and loop stability must be carefully analyzed, particularly if the motor and its load has significant inertia. As with most feedback systems, the loop will be stable when there is only one dominant pole. The loop filter time constant should preferably be at least 1 decade higher or lower than the constant of the motor and its load.

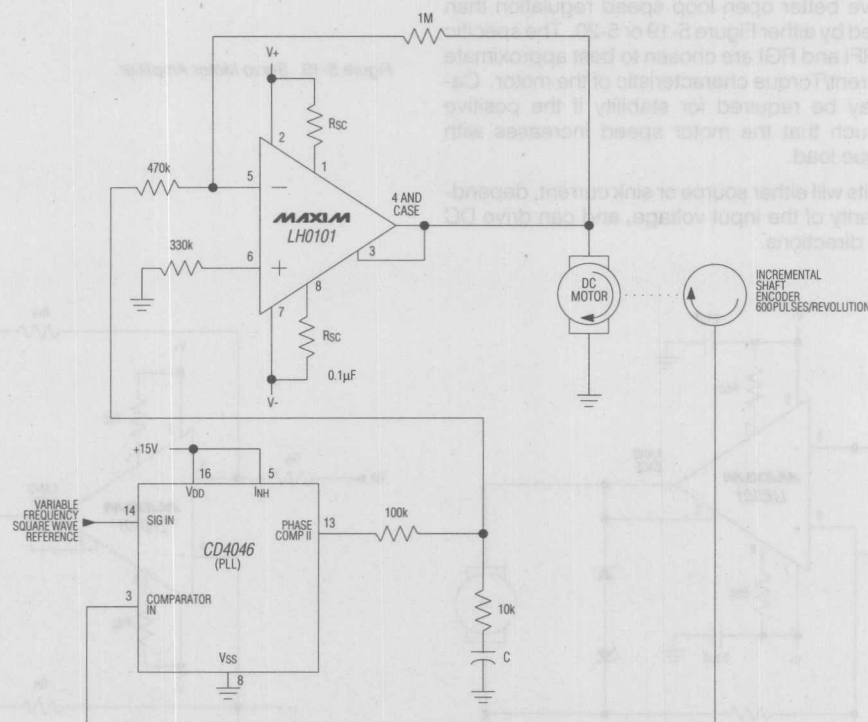


Figure 5-22. Servomotor Phase Locked Loop.

The 300kHz power bandwidth and 5 Amp peak output current capability of the LH0101 make it well suited for CRT yoke driver circuits. This circuit is basically a constant current source/sink with a transconductance of 435mA/V (reciprocal of the 2.3Ω current sense resistor). The resistor R_{DAMP} lowers the Q of the inductive yoke; the value of R_{DAMP} is chosen empirically for the least distortion at the operating frequency. At low frequencies R_{DAMP} is not required.

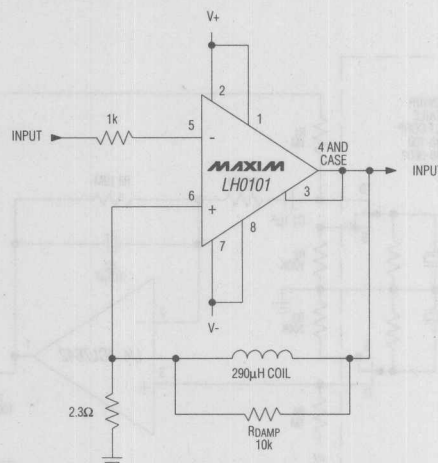


Figure 5-23. CRT Yoke Driver Circuit.

Remote IR Motion Detector With Only Two Wires

Penwalt Corporation has recently introduced a 180° Dual Channel Pyroelectric IR Detector Module (PIR 180-100). This module has two interdigitated sets of thin film IR detectors which are buffered by two internal J-FETs. A plastic Fresnel lens is available which not only concentrates the IR signal but also creates alternating zones of magnification which serves to enhance the effect of a moving target on the sensor.

The circuit shown in Figure 5-24 is a modification of the manufacturer's original recommended application circuit. This circuit is substantially smaller and is able to operate on less than 100 microamps of overall current. It may be used as shown in Figure 5-24 or a power MOSFET such as the IRF530 can be used in place of the R16, Q1 output stage.

Since the MAXIM ICL7642 Quad CMOS Op-Amp only requires 10 microamps per amplifier, the overall power consumption is reduced to such a low level that it is possible to derive the operating current through an external 5.1k ohm resistor with less than a 1/2 volt drop across the resistor. Figure 5-25 shows how the Figure 5-24 amplifier can be driven from a remote microcontroller through the external 5.1k ohm pull-up resistor. When the IR sensor detects a moving IR signal, such as the body heat of a human being, the output transistor turns on and shorts the two wires together. The microcontroller detects this logic "0" state and can initiate a warning signal. The circuit is capable of detecting the heat from a live person from 50 feet. However, the sensor will also respond to other sources of IR or temperature and, therefore, will be prone to cause false alarms if the sensitivity is adjusted too high.

The small size and low cost of this two wire driven sensor makes it very useful as a pre-warning of possible intrusion so that a TV camera or other device can scan the area.

The amplifier in Figure 5-24 consists of connecting the internal J-FET transistors as a X10 gain amplifier. The sensors are arranged to provide a dual output so that the ambient temperature inputs will be cancelled by the common mode rejection of the op-amp. The D.C. quiescent voltage may differ by several volts. Therefore, the second stage of amplification consists of a band pass filter which blocks the D.C. offset. The gain of the second stage is only 5 but this allows for a 1 microfarad monolithic capacitor to be used as the high-pass input to the amplifier. The passband is from around 0.1Hz to 2Hz. The next section of the amplifier shifts the output quiescent voltage to the internally generated reference voltage which is 1/2 the supply voltage. This state also serves as the variable "gain" stage. The last section uses two amplifiers as comparators to drive an "over-under" detector which drives an output device such as an open collector transistor.

Since the output of the IR sensor is A/C coupled to the amplifier, a steady input signal will result in a momentary output which clears as the signal equalizes the charge across the input capacitor. A second triggering of the alarm will occur when the detected person moves away from the view of the sensor.

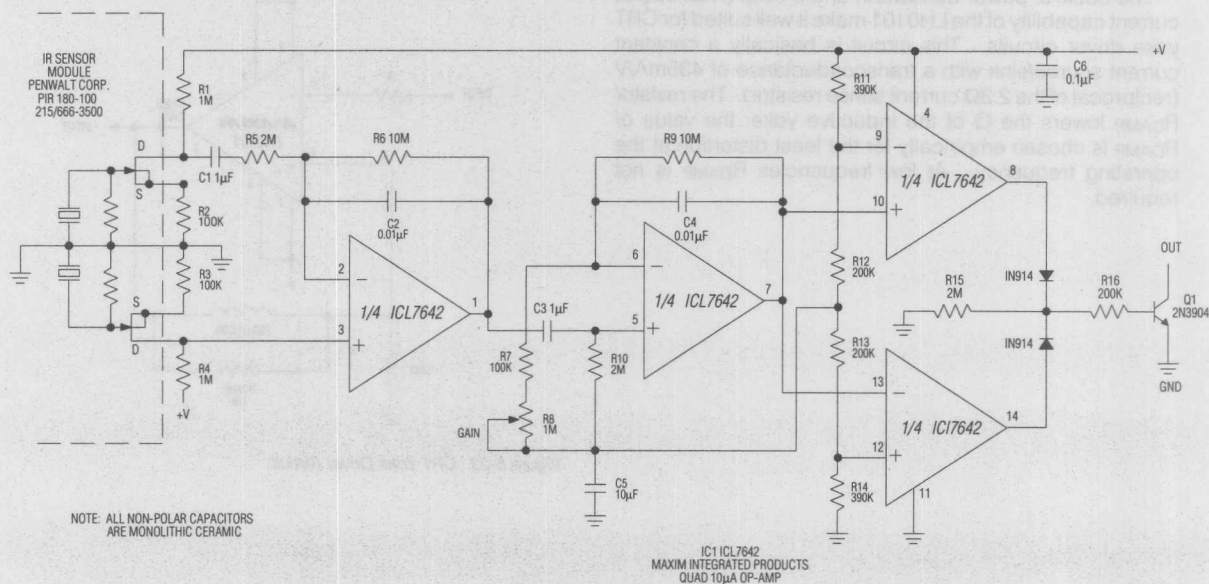


Figure 5-24.

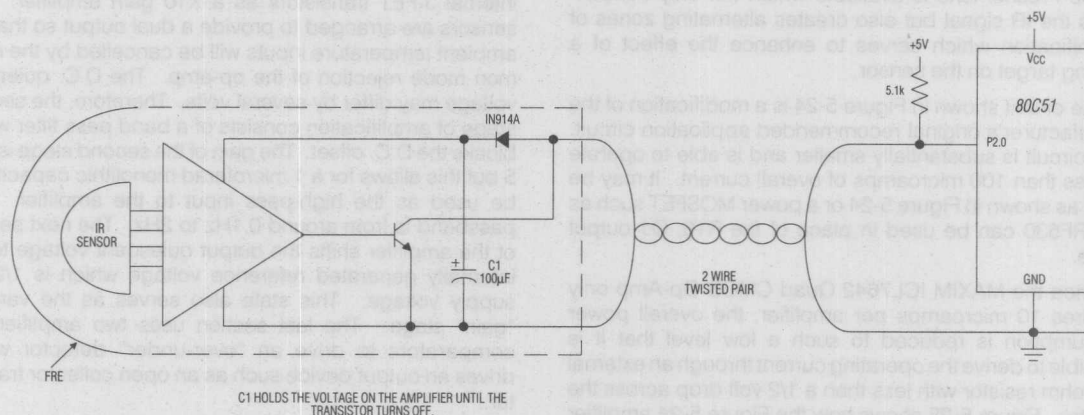


Figure 5-25.

The circuit below is used to test op-amp noise, and has an overall gain of 10,000. A gain of 1000, taken at the device under test (DUT), is followed by a gain of 10. The schematic differs from some common noise test circuits in that the measurement bandwidth used here extends to DC.

Noise specs are typically quoted from 0.1Hz to the upper limit frequency to stay away from offset drift with

temperature and 1/f noise. Offset drift and 1/f noise are usually lumped together because most real applications of precision op-amps are not afforded the luxury of separating the sources of low frequency error. Performance down to DC is what usually matters. Both bipolar and CMOS chopper amplifiers do very well when their strengths are utilized.

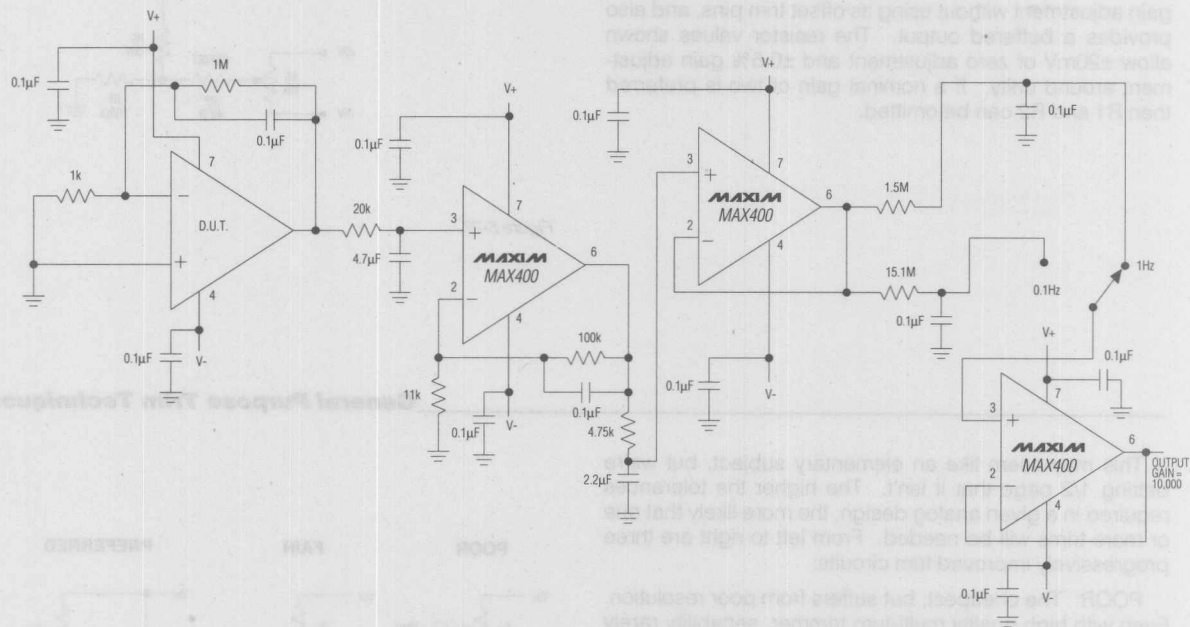


Figure 5-26.

A common error made in analog design is when overall system adjustments are "heaped" on the internal offset trim circuit of one op-amp. There are several reasons why this is usually not a good idea. One is that the amplifier's offset adjustment range may not be wide enough to remove errors from other circuits. Most op-amps' trim range is about two or three times their worst case offset spec. Another reason is that the drift performance of many op-amps degrades when their offset voltage is moved from the initial value. Some amplifiers specify this increased temperature drift in $\mu\text{V}/^\circ\text{C}$ per mV of adjustment, but many do not.

In this circuit, an op-amp takes care of both zero and gain adjustment without using its offset trim pins, and also provides a buffered output. The resistor values shown allow $\pm 20\text{mV}$ of zero adjustment and $\pm 0.5\%$ gain adjustment around unity. If a nominal gain of two is preferred then R1 and R2 can be omitted.

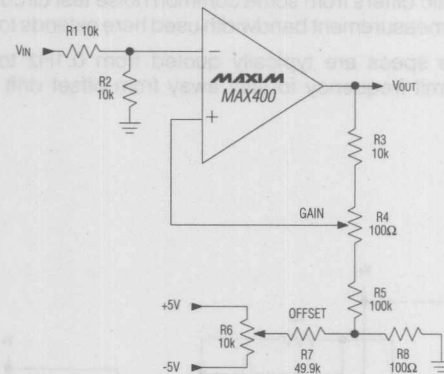


Figure 5-27.

General Purpose Trim Techniques

This may seem like an elementary subject, but we're betting 1/2 page that it isn't. The higher the tolerances required in a given analog design, the more likely that one or more trims will be needed. From left to right are three progressively improved trim circuits:

POOR: The cheapest, but suffers from poor resolution. Even with high quality multi-turn trimmer, settability rarely is better than 1%. Also the temperature drift of most trim pots will not support precision work with this approach.

FAIR: This is the common "first-pass" at improving drift and resolution. The range of the trimmer is reduced by fixed resistors (hopefully 1%) so the resolution is increased, but a drawback is that it often requires low resistance trimmers (below 100Ω) which are frequently difficult to obtain. Another disadvantage is that absolute value drift in the trim pot will affect the output. On most trimmers, absolute drift has very loose limits compared to ratio drift.

PREFERRED: By adding one more resistor (R3), the problems of the center circuit are eliminated: 1) Large resistance values can be used for the trimmer. 2) Absolute trimmer drift has no effect on the output. 3) The adjustment will have highest resolution in the center of range where it is needed most. 4) The design can start with the optimum fixed resistor divider values, which needed not be changed if the trim is added later.

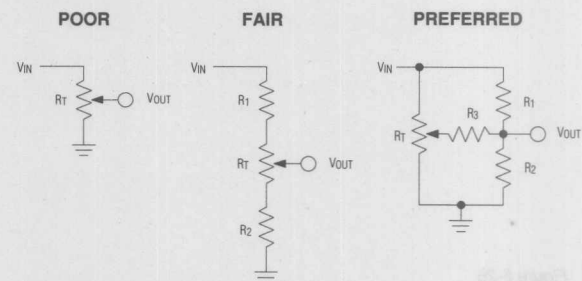


Figure 5-28.

(Reprinted with permission from Vishay Corp. San Diego, CA)

Gain setting resistors must be chosen so that the operational amplifier performs to expectation without unwanted amplification drift or noise insertion.

Noise

Resistors whose current paths include particle to particle contact points of conductive material in a non-conductive matrix introduce current noise to varying degrees depending on construction and ratio of conductive to non-conductive material. (Higher values have less conductive material, and high noise insertion.) Composition resistors (conductive carbon in non-conductive plastic) will insert -8 to +12dB of current distortion or noise and cermet resistors (conductive metal in non-conductive glass) will insert -26 to -12dB.

Resistors made of metal alloys where the resistivity is at the intergranular boundaries and these boundaries are collectively very long do not insert measurable noise. (-42 to -36dB is below the measurement capabilities of most equipment and below the requirements of most circuits.) Resistors made of rolled foil (Vishay) and resistors made

of drawn wire (Vishay and others) do not insert measurable noise.

Resistors characterized as "thin film" (Vishay and others) are produced from such a variety of materials and processes that it is well to request the noise index from the manufacturer prior to approval of a candidate thin film resistor.

Amplification Drift

The amplifier will maintain its gain only to the degree that the external resistors maintain their value and ratio. Resistors drift to varying degrees depending on construction, value range, and severity of stress. If the stresses are differently applied to one of the gain setting resistors then the gain can be temporarily or permanently distorted. Stresses of temperature, voltage, frequency, chemical abuse, mechanical abuse, and time all affect resistors and/or ratio. Devices with other than copper leads introduce ratio changes due to the thermal EMF generation at the lead to PC board junction.

All of the above potential for drift can be minimized to the degree required from selection of the proper resistor pair (or quad in the case of a differential amplifier). In order of performance, the candidate resistors are shown in Table 5-3.

Table 5-3.

A 25ppm/°C	Thin Film Resistors (discrete)	For: Cost, board layout, can select power rating to favor dissipation, quiet. Against: No way to unify temperature.
B 100ppm/°C	Thick Film (Cermet) DIP or SIP	For: Cost, uniform temperature Against: Noise, high TCR, time and temperature drift.
C 10ppm/°C	Wirewound resistors (discrete)	For: Stable, good TC, good noise. Against: Size, inductive/capacitive.
D 10ppm/°C	Thin Film networks DIP or SIP	For: Uniform temperature, any resistance combination. Against: Mask making causes long lead time.
E 5ppm/°C	Foil resistors (discrete)	For: Ultra stable, temperature differences not so important. Against: Cost.
F 5ppm/°C	Foil dividers 3 lead SIP	For: Ratio accuracy to 0.005%, TCR tracking to 0.5ppm/°C. Against: Cost, possible mask making time.
G 5ppm/°C	Foil Networks (Hermetic)	For: Any resistance combination, no mask making time, no minimum quantity, best long term stability. Against: Cost, resistance range.

Some simple rules that apply to all resistor ratios are:

1. The lower the fundamental TCR the better the feed-back resistor will track the input resistor.
2. The smaller the amplification ratio the better the track.
3. The lower the dissipation the better the track.
4. The higher the technology the better the track.
5. Networks track better than discretes of the same technology.
6. The lower the specification the less the cost.

For further assistance in resistor selection contact the application engineering departments of the various resistor manufacturers.

A MAX329 low leakage multiplexer conveniently switches gain in an instrumentation amplifier circuit. R1 through R7 set the range of possible gains. The values shown provide gains of 1, 2, 4, and 8. Gain accuracy and common-mode rejection are dependent on resistor matching accuracy, but are independent of multiplexer on-resistance.

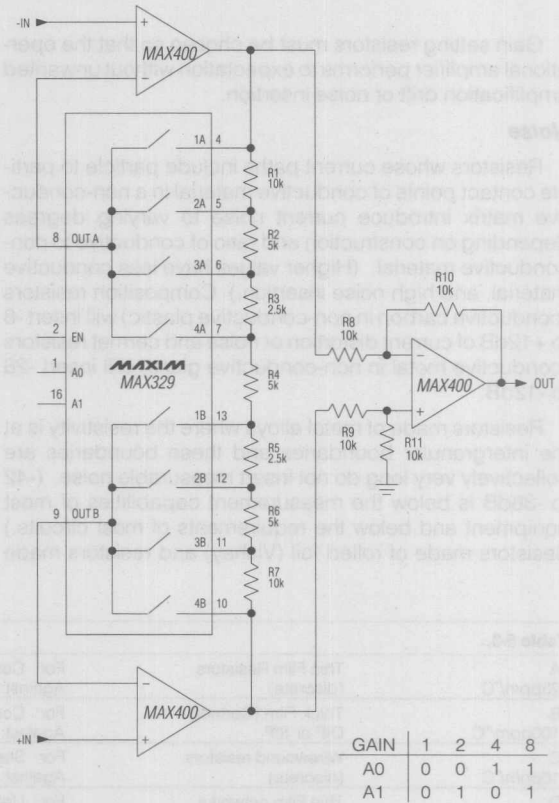


Figure 5-29.

Differential To Single-ended Converter

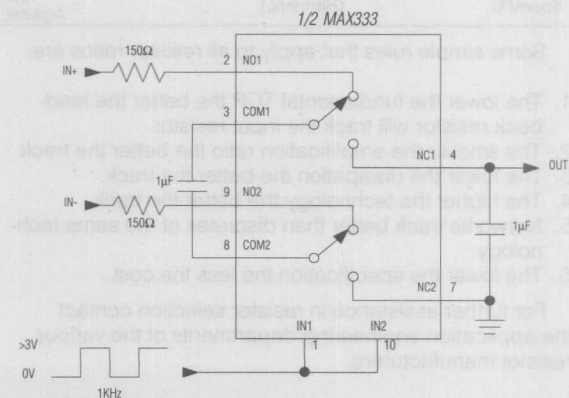


Figure 5-30.

Submultiplexing Minimizes Leakage

Recognizing that leakage current is a critical analog switch specification, Maxim guarantees an OFF channel leakage of only 0.1nA (only 1/100 of the industry standard spec) and ON channel leakage of 0.2nA (1/50 of industry standard spec). This may still be too much leakage current if many channels are bussed together as shown in the left side of this figure.

Submultiplexing as shown on the right hand side will reduce the total system leakage. Another benefit is that the digital interface is simplified since no chip-enable decoders are needed.

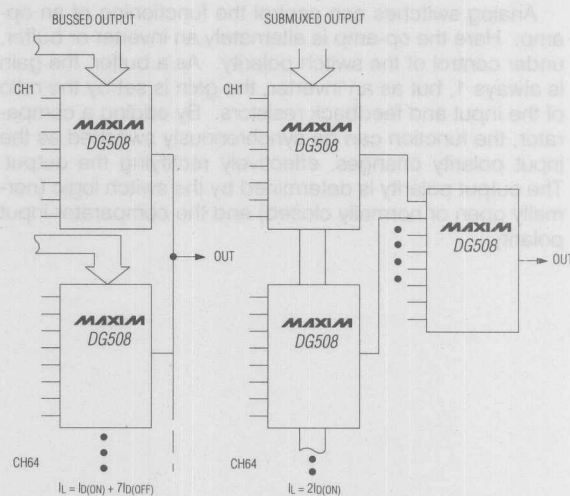


Figure 5-31.

Demultiplexing A 16-Bit DAC

Two DG508As can be combined with low cost buffer amplifiers to generate eight 16 bit accuracy outputs from one 16 bit DAC.

The upper DG508A routes the DAC output to 1 of 8 sets of voltage-hold capacitors and buffers. The lower DG508A closes a feedback loop by selecting the appropriate buffer output. The DAC output amplifier will drive the hold capacitor such that the buffer amplifier output is equal to the DAC output. The buffer amplifier V_{OS} therefore is not critical, and the buffer need only be low leakage to reduce the "voltage droop" while the other channels are being updated. The amplifier at the output of the DAC should be a high quality amplifier with both low V_{OS} and V_{OS} tempco.

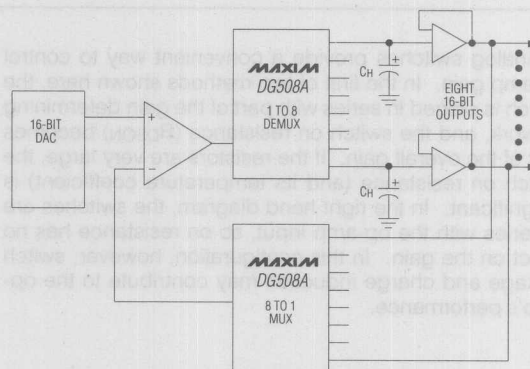


Figure 5-32.

Analog switches can control the functioning of an op-amp. Here the op-amp is alternately an inverter or buffer, under control of the switch polarity. As a buffer, the gain is always 1, but as an inverter, the gain is set by the ratio of the input and feedback resistors. By adding a comparator, the function can be synchronously switched as the input polarity changes, effectively rectifying the output. The output polarity is determined by the switch logic (normally open or normally closed) and the comparator input polarity.

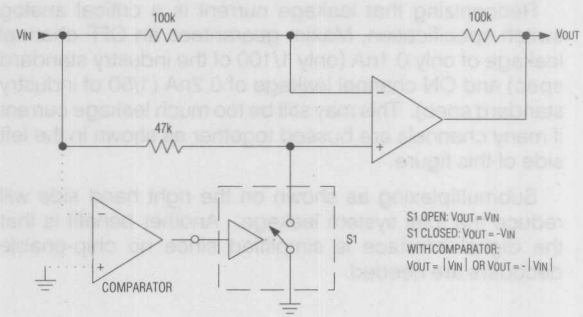


Figure 5-33.

Op Amp Gain Switching Techniques

Analog switches provide a convenient way to control op-amp gain. In the first of two methods shown here, the switch is placed in series with part of the gain determining network, and the switch on resistance ($R_{DS(on)}$) becomes part of the overall gain. If the resistors are very large, the switch on resistance (and its temperature coefficient) is insignificant. In the right hand diagram, the switches are in series with the op-amp input, so on resistance has no effect on the gain. In this configuration, however, switch leakage and charge induction may contribute to the op-amp's performance.

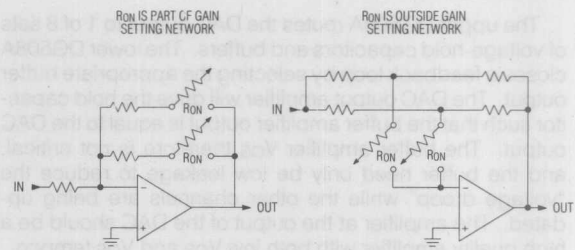


Figure 5-34.

The on resistance or $R_{DS(on)}$ of an analog switch varies with both the power supply voltages and the analog input voltage. In both cases the $R_{DS(on)}$ varies because the V_{GS} (gate-to-source voltage) changes.

The MAX331 uses an N-channel and a P-channel MOSFET in parallel. When the analog signal voltage approaches the $V+$ supply voltage, the V_{GS} on the N-channel MOSFET is reduced and its resistance goes up. A similar effect occurs when the input voltage approaches $V-$, but the increase in $R_{DS(on)}$ is less since the N-channel MOSFET is fully turned on and its resistance is less than that of the P-channel MOSFET.

This graph also applies for: MAX332, MAX333, DG201A, DG202, DG211, and DG212. Other Maxim analog switches and multiplexers behave similarly, with proportional differences to resistance values. Exceptions are MAX310/311, MAX341/3/5/8, MAX358/359, MAX368/369, and MAX378/379, which have different internal switch topologies.

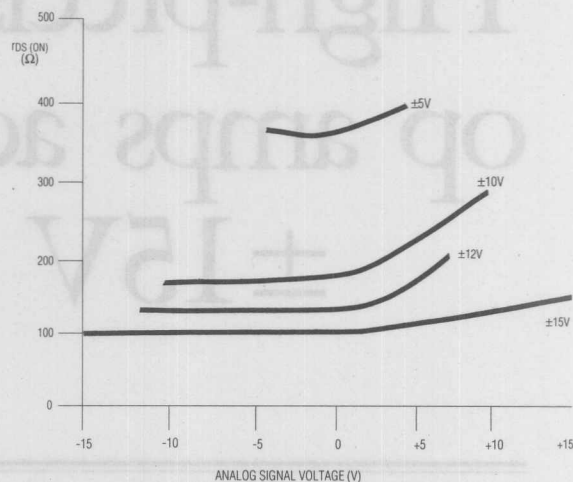


Figure 5-35.

High-precision CMOS op amps accommodate $\pm 15V$ supplies

Monolithic, dc-stabilized CMOS amplifiers are no longer limited to a $\pm 8V$ power-supply range: One family of CMOS op amps can operate from $\pm 15V$ supplies. The op amps' wider supply range makes them suitable for use in a variety of analog systems that require precision dc amplification.

Leonard Sherman,
Maxim Integrated Products

By employing a family of chopper-stabilized CMOS op amps (the MAX420 Series) that can operate from ± 2.5 to $\pm 16.5V$ supplies, you can obtain precision dc amplification in industrial-control, data-acquisition, servo, and other applications that were beyond the capabilities of earlier CMOS chopper-stabilized op amps.

These precision amplifiers can provide good signal conditioning for thermocouples, for example. Despite their advantages—low cost, high reliability, and the ability to measure wide temperature ranges—thermo-

couples are somewhat difficult to deal with electrically, because they have low output signal levels and require an ice-point reference. Typical thermocouple output signal levels (on the order of tens of microvolts per degree C) dictate that the signal-conditioning amplifiers used with thermocouples must have input offset and drift specifications well below those levels. You need such specs especially if you want to realize resolution and repeatability to a fraction of a degree.

The circuit in Fig 1 readily amplifies thermocouples' low-level output signals. The MAX422 has a maximum input drift spec of $50 \text{ nV}/^\circ\text{C}$, so the amplifier contributes only 0.001° of output error for each degree of shift in ambient temperature. Because the op amp can use $\pm 15V$ power supplies, the design is simple: A basic inverting summing network combines the thermocouple output, cold-junction compensation, and cold-junction offset.

The trim procedure is also very simple, because gain and cold-junction adjustments don't interact. This lack of interaction is a significant advantage in multichannel setups, which are fairly common in thermocouple measurement systems.

The small-signal npn transistor provides ice-point compensation for the thermocouple. It generates a

Signal-conditioning amplifiers used with thermocouples must have input offset and drift specifications well below typical thermocouple output signal levels.

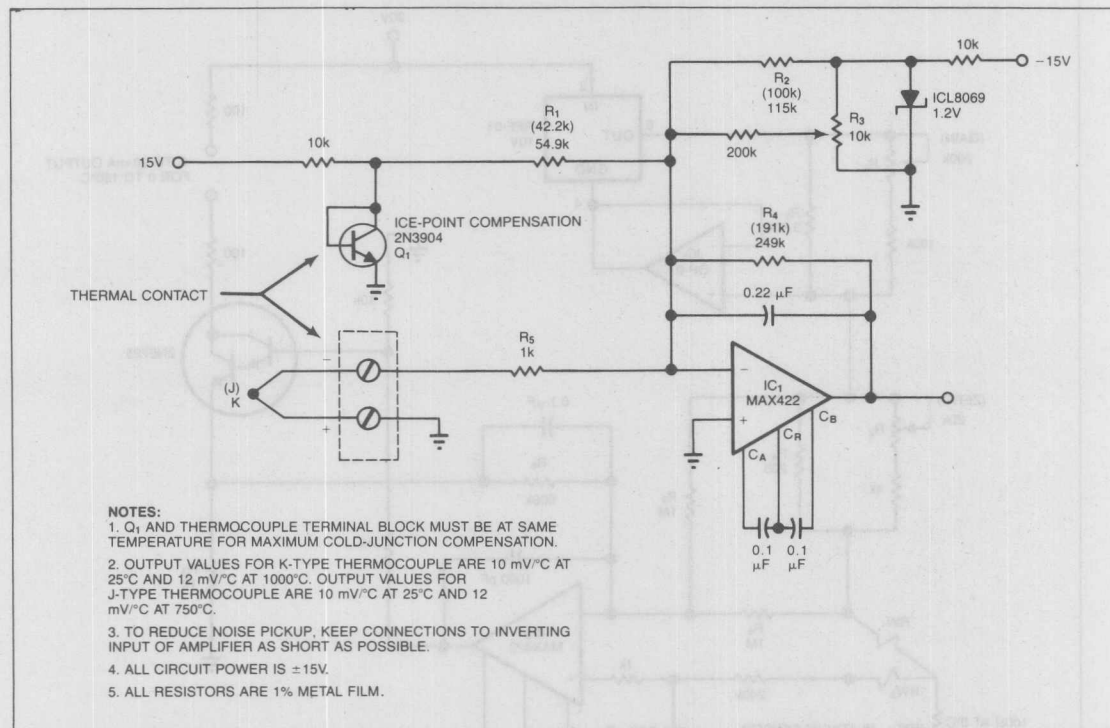


Fig 1—This simple signal-conditioning circuit uses an inverting summer to combine thermocouple output, cold-junction compensation, and cold-junction offset signals. The circuit is easy to trim, because the gain and cold-junction offset adjustments do not interact.

–2.2 mV/°C signal, which cancels the thermoelectric error signals generated at the thermocouple's input terminal strip. You should place the transistor as close as possible to the terminal block; to achieve optimum performance, you need to effect thermal contact between the devices.

For temperatures below 200°C (with a common type K thermocouple), the circuit in Fig 1 provides a 10 mV/°C output. The circuit includes no linearization, so this output factor will change at higher temperatures—12 mV/°C (for type K thermocouples) at 1000°C. Although the circuit component values shown are for J- and K-type thermocouples only, the circuit can accommodate other types of thermocouples. To provide gain and cold-junction compensation, you simply have to calculate new values for R_1 , R_2 , and R_4 .

Platinum resistance thermometers (PRTs) present another classical transducer-conditioning problem. By using platinum wire as the sensing element in a PRT,

you can achieve very high accuracy and repeatability over a wide operating-temperature range. As a result, PRTs are well suited for high-accuracy thermometry applications. Like thermocouples, PRTs have a major drawback, however: They provide a low-level output signal. Although the change in resistance over temperature of platinum wire is very predictable, it's also very small (0.3815%/°C), so you'll require large precise gain and long-term stability in order to develop a useful output.

The PRT amplifier circuit in Fig 2 uses a 3-terminal sensing scheme to eliminate errors from lead resistance, so you can remotely locate the sensor. In addition, the circuit design refers the sensor output to ground, thus minimizing noise-pickup problems. With a 30V supply, the circuit provides a 4- to 20-mA current output with compliance from 3 to 28V.

The REF-01 10V reference combines with IC₁ to generate a precise constant current that biases the PRT

and also creates fixed voltages for sensor-offset correction and wire-resistance error cancellation. Lead-resistance effects (RW_1 , RW_2 , and RW_3) are subtracted from the real temperature signal at the input of the PRT amplifier, IC_2 . The circuit in Fig 2 works on the principle that the resistance of all three leads will be identical. The lead-resistance effects related to RW_2 are insignificant, however, because only op-amp bias cur-

rent passes through RW_2 .

The temperature and correction signals sum at IC_2 as follows: The voltages on the PRT and its ground wire (RW_3) are amplified by 1, the voltage drop on the PRT's positive lead (RW_1) is amplified by $-\frac{1}{2}$, and the drop across R_4 (an offset resistor) and RW_1 is amplified by $-\frac{1}{2}$. As a result, the RW terms cancel, and the net output appearing across R_3 is the PRT voltage minus $\frac{1}{2}$

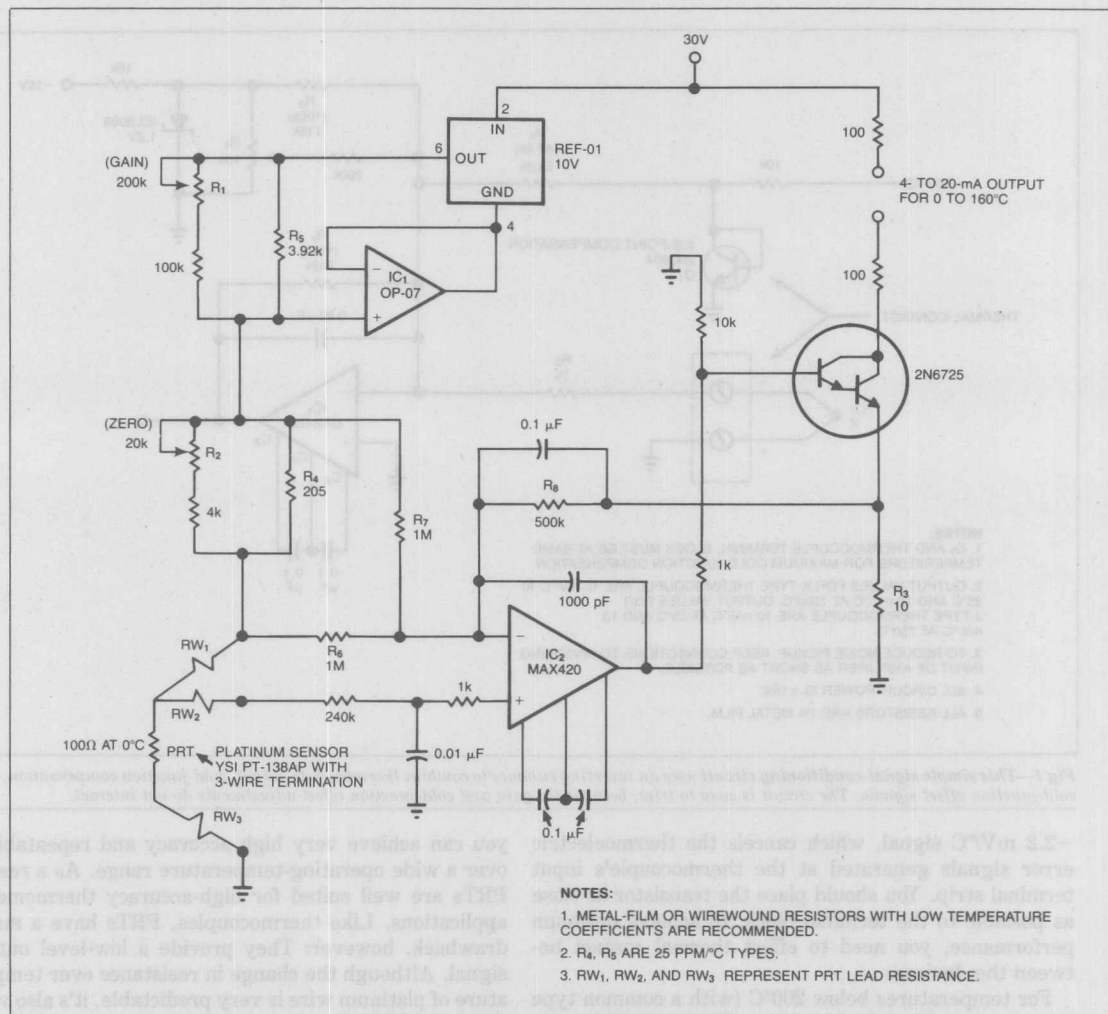


Fig 2—By referring the sensor to circuit ground, this platinum-resistance-thermometer amplifier circuit minimizes noise-pickup problems. Because the circuit uses a 3-terminal sensing scheme to eliminate errors from lead resistance, you can remotely locate the sensor.

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the offset on R_4 . IC_2 drives a Darlington transistor (Q_1); R_3 senses Q_1 's output current to provide a feedback signal for IC_2 .

To calibrate the circuit, you must adjust R_2 and R_1 . R_2 trims the sensor's offset, and R_1 handles circuit gain adjustments. If you adjust the offset first, the gain trim will not interact, so you can probably make each adjustment in only one pass.

Better precision for instrumentation amps

Precision amplifiers are usually a necessity in applications involving bridge measurements (strain gauges, load cells, and some types of pressure transducers), because these applications require high accuracy and low signal levels. In most cases, instrumentation amplifiers can easily handle the 30-mV differential output signals from these bridge-type devices. These instrumentation amplifiers have finite, controllable, differential gain that's fixed or that can be set with one or two resistors.

The high-performance instrumentation-amplifier circuit in Fig 3 amplifies a small differential signal from a

strain-gauge bridge into a large ground-referenced signal. Such a configuration is typical of off-the-shelf instrumentation amplifiers; however, when you use MAX421 amplifiers in the front end, the offset and drift performance you obtain is better by an order of magnitude than that available in off-the-shelf amplifiers.

As with all instrumentation amplifiers employing this 3-stage configuration, the front-end and output amplifiers will both affect overall drift performance. The output amplifier's effect on drift (referred to the input) is divided by the front-end gain, which is approximately 30 (the overall gain is 300). The MAXOP07's V_{OS} specifications ($75 \mu V$ and $1.3 \mu V/^\circ C$) are divided and added to two times the MAX421 error, yielding a maximum input-referred error of $12.5 \mu V$ and $0.15 \mu V/^\circ C$. Even when front-end gain is set at 30, the MAXOP07 contributes more to offset error than do the MAX421s.

The chopping circuits of the front-end op amps are locked together via their clock-control pins. IC_1 's INT/EXT clock pin is unconnected, so it operates from its internal 400-Hz clock in normal fashion. The CLK IN pin of IC_1 functions as an output. Since IC_2 's INT/EXT

Addressing thermal problems

In an instrumentation amplifier circuit—as in any design dealing with low-level signals—the quest for microvolt-offset and nanovolt-drift performance involves more than just selecting a high-precision amplifier. When you're trying to amplify low-level signals, any number of outside error sources can complicate your task. These errors are troublesome because it's very hard to distinguish them from real signals or amplifier error.

Thermoelectric voltages provide a perfect example of such error sources. The same phenomenon responsible for thermocouple operation can generate significant errors at pin-to-socket, socket-to-board, and board-to-edge-connector interfaces, and even at soldered connections. The level of the voltage gener-

ated in such situations can range from one-tenth to tens of microvolts per degree C. In general, designers deal with this problem by minimizing the use of sockets and connectors in low-level circuitry, or by using components designed for low thermal EMF.

Although temperature obviously contributes to thermoelectric errors, thermal gradients in low-level circuitry cause more problems than does the mere presence of heat. Gradients can, for example, cause the normally balanced input connections of a sensitive amplifier to be at different temperatures. These connections then generate different values of thermoelectric voltages that the amplifier's inputs can no longer completely cancel; the final output is an offset error. The most effective way to com-

bat thermal gradients is to keep power dissipation low and minimize air currents in and around low-level circuitry and connections.

You can also solve thermoelectric voltage problems by designing thermal symmetry into the circuit layout. This solution can involve adding dummy resistors and connections so that the thermal mass—as well as the number of thermoelectric error sources in an input pair—will cancel. In addition, you might have to run input traces close to each other and keep their dimensions identical. You might also find it helpful to develop some thermal filtering by minimizing enclosure size, or by insulating sensitive areas.

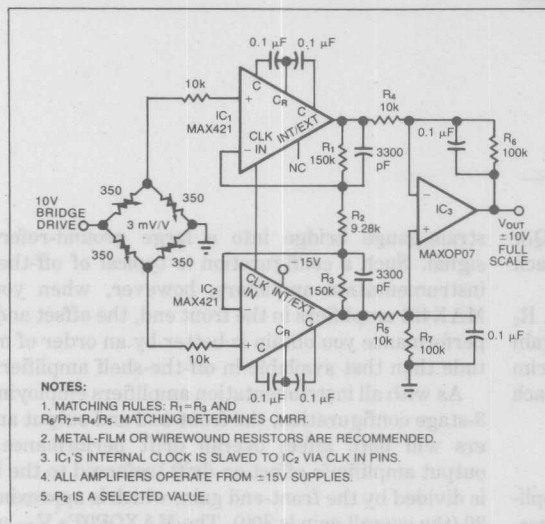


Fig 3—To eliminate the low-level errors caused by clock interaction, this instrumentation-amplifier circuit locks the chopping circuits of the two front-end op amps together.

CLK pin is connected to the negative supply, its clock is disabled. IC1's CLK IN terminal drives IC2. By synchronizing the input amplifiers in this manner, you eliminate low-level errors caused by clock interaction.

Gain-setting resistor matching limits the amount of common-mode rejection that you can realize. For prototype or test purposes, you can generally achieve 0.1 to 0.01% matching when you use selected 1% resistors. For more precise matching, you'll have to use resistor arrays or resistors that have low temperature coefficients and tighter tolerances. Once you've satisfied your rejection needs, you can adjust R_2 to change overall circuit gain without affecting common-mode-rejection performance.

Amplifying high-level signals

If you're designing circuitry to handle high-current measurements, you'll typically need to use sense resistors, so you'll have to contend with increased power-supply source impedance, and possibly even high power dissipation. Because it uses a low-offset amplifier in a high-current application, the circuit in Fig 4 eliminates these concerns.

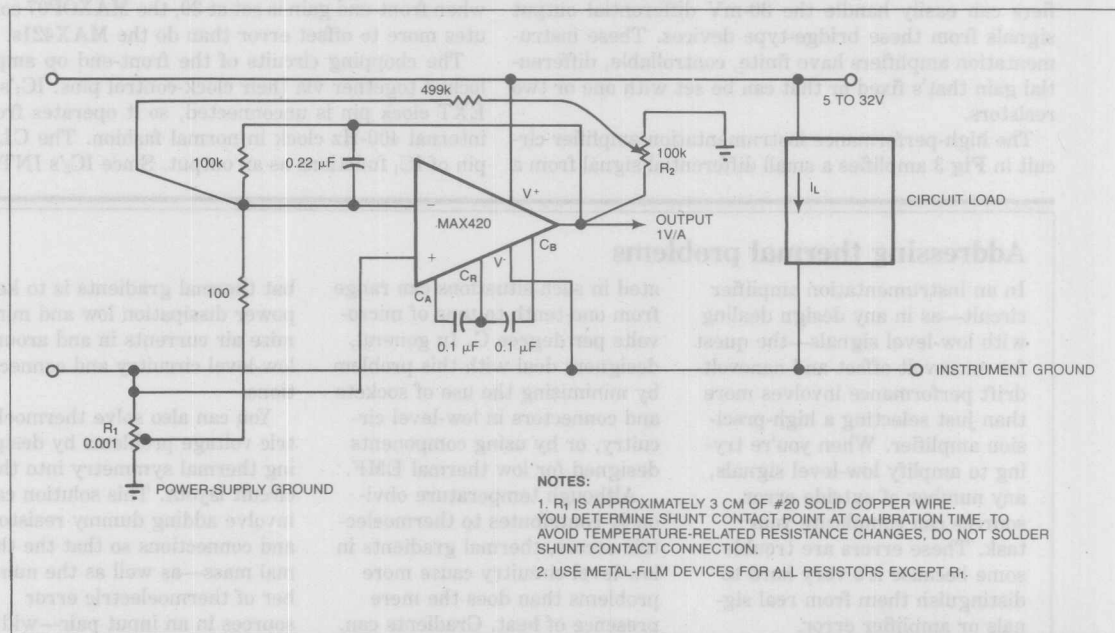


Fig 4—You can make sense measurements without disturbing the operating load circuitry in this current-sense amplifier circuit because of the low offset specifications of the MAX420 op amp.

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Although temperature obviously contributes to thermoelectric errors, thermal gradients can cause more problems than can the mere presence of heat.

The MAX420 is suitable for this circuit for two reasons: First, because of the MAX420's low offset-voltage specification, you can use a low-value sense resistor (0.001Ω in Fig 4). The current measurement will, therefore, have no adverse effects on the operating load circuitry. Second, the MAX420 has a common-mode input range that includes the negative supply, which is circuit ground in this case. When the input range includes ground, the op amp can read the current-sense voltage across R_1 without the need for level shifting. Further, the MAX420 allows the circuit to operate from supply voltages of 5 to 33V.

In Fig 4, the sense resistor is actually a short piece of solid copper wire with a movable tap. To calibrate the circuit, you apply a known full-scale current and use the tap as a coarse trim to establish the proper output voltage. You then adjust R_2 to set amplifier gain and develop the precise output-voltage level. If you solder the tap on R_1 , be sure to wait until the connection cools completely before you make the fine trim; this way, you'll avoid introducing errors caused by any change in wire resistance at high temperatures.

The circuit in Fig 4 requires no offset adjustments. With the values shown, the circuit delivers 1V per amp

of supply current. You can, however, change the sense-resistor value or the amplifier gain to develop other output ranges. With a 10A supply current, the load will experience a shift in ground potential of only 10 mV, and the sense resistor will dissipate only 0.1W.

You don't need to limit monolithic chopper amplifiers to applications involving low-level signal amplification. Because devices like the MAX420 perform precise amplification, you can use them not only in the primary signal path, but also to stabilize other circuitry. In effect, this approach lets you use CMOS op amps to improve the dc performance of wide-bandwidth or high-power circuitry.

The high-speed 12-bit power D/A converter shown in Fig 5a provides a good example of such an application. This circuit uses an LH0101 power op amp (300-kHz power bandwidth and 2A drive capability) as an output stage. The LH0101 has a 15-mV offset-voltage specification, so it can't accommodate 12-bit converter resolution by itself. The MAX421 overcomes the problem by monitoring the LH0101's inverting input and driving the noninverting input so that the summing junction is at 0V (to within $5\mu\text{V}$, the 421's error spec). The result is a high-speed, no-drift DAC circuit.

The MAX421 can use the same power supplies as do the LH0101 and AD565. The voltage divider at the MAX421's output attenuates the LH0101's correction signal to avoid any overdrive problems. Addition of the offset correction has no noticeable effect on the circuit's dynamic performance. Fig 5b shows step responses obtained with and without the correction circuitry in operation. The stabilized and unstabilized waveforms exhibit no perceptible slewing or settling-time differences as a result.

Maximize voltage calibrator performance

To design a voltage calibrator that can generate a 0 to 10.0000V output with $100\mu\text{V}$ resolution (Fig 6), you must use an op amp with very good offset, drift, and common-mode rejection specs. Although the circuit is designed for reliable absolute-reference stability, it has a ratiometric capability: Both fixed and variable references, based on the same source, are available simultaneously. Such a feature is especially useful in applications involving linearity checks of digital voltmeters or A/D converters. In such cases, relative rather than absolute results have the most significance. Very few off-the-shelf calibrators, if any, provide this dual-reference feature, so if you want such a feature you must build your own calibrator.

MAX420 amplifiers

MAX420 Series amplifiers offer very low zero-offset and zero-offset-drift specifications ($5\mu\text{V}$ and $0.05\mu\text{V}/^\circ\text{C}$, respectively). The parts can operate over a 5V (or $\pm 2.5\text{V}$) to 33V (or $\pm 16.5\text{V}$) supply-voltage range. In addition, input bias current for the op amps specs at only 30 pA.

The amplifiers provide low-power operation at any supply voltage, and they offer FET-type bias currents (30 pA) for high-impedance measurements. The series also includes two devices (MAX422 and MAX423) that draw only 25% of the supply current that the standard parts draw, but that don't sacrifice dc performance. The two parts do, however, exhibit some decrease in bandwidth and output drive capability.

The 8-pin versions of the family are compatible with standard op-amp footprints with respect to inputs, outputs, and supply lines. To enable the amplifiers, you simply connect two external capacitors to the pins that conventional amplifiers normally use for offset trimming.

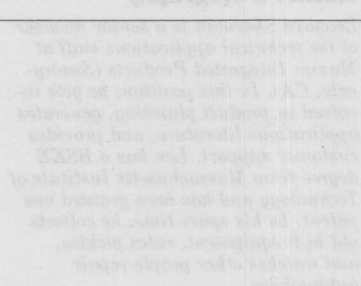


Fig 6's circuit uses an AD2710 voltage reference, which the manufacturer can trim to within 1 mV. If you're going to use the circuit for purely ratiometric measurement, a 1-mV (or even larger) error, and some degree of drift, will cause few problems. For absolute calibration applications, however, you'll require an accurate, low-drift reference. You can adjust the 2710 for a tighter tolerance by using a 10-k Ω multiturn trimmer, as shown in Fig 6.

IC₁, an MAX420 connected as a precision unity-gain inverter, provides a negative version of the reference voltage that's adjusted with trimmer R₆. Special reed relays, designed for minimal thermal EMF errors, select either the positive or the negative reference to drive the fixed and variable outputs.

It's not a good idea to use a conventional switch to perform the polarity-select function, because conventional switch contacts generate small thermoelectric voltages. These voltages can introduce significant errors when the output resolution is as low as 100 μ V/step, as it is in Fig 6. By using four relays, you can select the polarity of the fixed and variable outputs independently.

A Kelvin-Varley voltage divider (R₅), with five decades of adjustment range, divides the fixed reference, developing output increments as small as 100 μ V with 20-ppm linearity. The fixed and variable output buffers (IC₂ through IC₅) are composites of MAX420 op amps and LH0101 buffers. This combination provides reasonably good output current drive, and it has less than 10 μ V of untrimmed error from offset, common-mode rejection, and other sources.

EDN

Author's biography

Leonard Sherman is a senior member of the technical applications staff at Maxim Integrated Products (Sunnyvale, CA). In this position, he gets involved in product planning, generates applications literature, and provides customer support. Len has a BSEE degree from Massachusetts Institute of Technology and has been granted one patent. In his spare time, he collects old hi-fi equipment, rates pickles, and watches other people repair automobiles.



Multiplexer-amp combo tames losses in wideband circuits

Greg Schaffer

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By making a slow CMOS op amp simulate a much faster bipolar one, a multiplexer-amplifier chip drives TV-camera switching chains.

Teleconferencing cameras, flash converters, video crosspoint switches, and attenuators can make good use of a monolithic video multiplexer chip with zero insertion loss, low input capacity, and 75- Ω line-driving capability. But such a chip—a multiplexer driving an op amp near unity closed-loop gain—did not exist until quite recently.

The problem is that putting the multiplexer and op amp on the same chip presented some difficult trade-offs: a CMOS multiplexer is best for switch-

ing with minimal power consumption, and a bipolar op amp is best for maximum gain-bandwidth product. So an all-bipolar chip with diode bridge multiplexer switches, for example, would need a lot of power, but an all-CMOS chip of conventional design would be too slow.

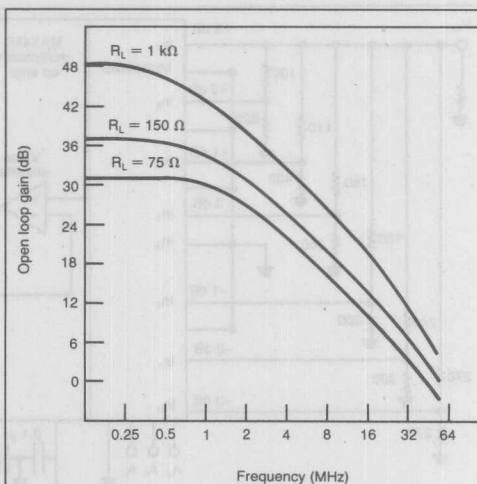
The conventional solution—relying on two separate chips, say a 200-MHz CMOS multiplexer and a 100 to 300 MHz bipolar op amp—is both difficult and not very cost-effective. It is difficult to stabilize a very wideband op amp near unity closed-loop gain, and it is wasteful of bandpass.

Similarly, wideband multiplexers are all designed with low resistance (R), typically 50 Ω , to directly drive low impedance (75- Ω) cables without an amplifier. This low R means high channel capacitance (C), as much as 50 pF, which typically might limit the bandpass to 50 to 100 MHz because of input RC rolloff. Opting for a multiplexer with higher R and lower C —assuming one was available—would not be of much help. With the multiplexer and op amp only 0.25 in. apart, 2 to 3 pF of stray wiring capacitance would still limit the bandpass.

A monolithic solution to this designer's dilemma is Maxim's MAX455, a 50-MHz, 250 mW, $\pm 5V$, eight-channel multiplexer-amplifier. Other versions have four and two channels as well as the bare

video amplifier, the MAX454, 453, and 452, respectively. While there are some TV applications in which a separate bipolar op amp and a special multiplexer may be necessary, the all-CMOS device supplies low input loading, easy stabilization against oscillation, and general cost-effectiveness.

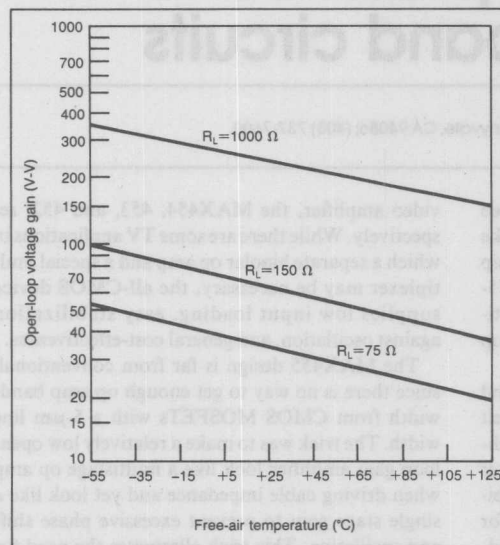
The MAX455 design is far from conventional, since there is no way to get enough op amp bandwidth from CMOS MOSFETs with a 5- μm line width. The trick was to make a relatively low open-loop gain amplifier look like a multistage op amp when driving cable impedance and yet look like a single stage gain to prevent excessive phase shift and oscillation. This trick eliminates the need for phase compensation to prevent oscillation at low closed-loop gain. Without the need for compensation, the bandpass of the device is improved by a factor of 2 to 10 or more. However, voltage gain will



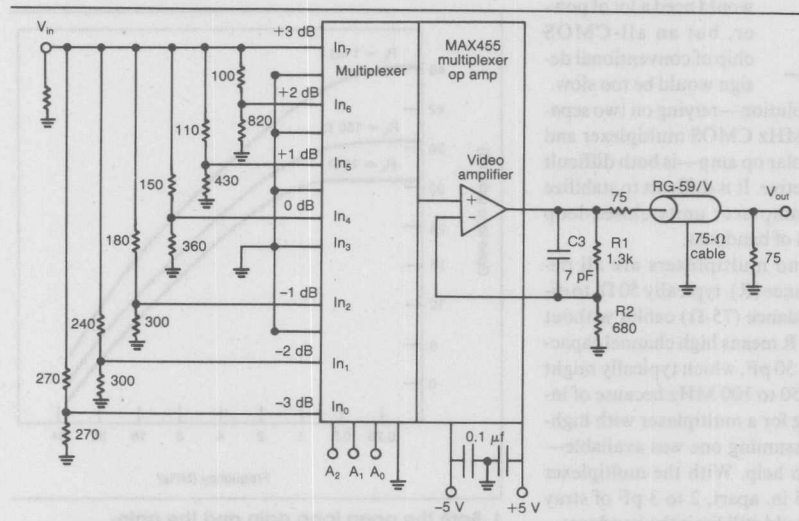
1. Both the open loop gain and the gain-bandpass increase with load, which becomes apparent when the MAX455, configured as an instrumentation amplifier with a 20-dB closed loop gain, drives a 1- $k\Omega$ load. The gain-bandpass product is 150 MHz.

be proportional to load resistance.

So instead of three amplifier stages (typical of an op amp) there are just two: a 38 V/V differential input stage driving a push-pull transconductance output stage with



2. The gain of MOSFET transistors, however, drops with increasing temperature. A MAX455 chip with a closed-loop gain of 6 dB and driving a 150- Ω load would lose 1% of its gain when operating at +85°C instead of +25°C.



3. This video amplifier-attenuator has 25-MHz typical bandpass and 70 dB off-channel isolation in the TV band. It provides seven steps from -3 to +3 dB in 1-dB increments, plus a no-output position. The resistors R1 and R2 set a gain of 9 dB, 6 of which cancel out the 6-dB loss in driving the back-terminated cable. C3 reduces peaking caused by the amplifier input capacity.

the help of current mirrors for biasing. The output stage has gain proportional to output R and equal to unity with a 75- Ω load. The low gain is not a drawback, since the amplifier usually runs at a closed-loop gain of 0 or 6 dB; its dc transfer function is quite linear, and it is always driving a well-defined resistive load. The amplifier also behaves like a true op amp in terms of low drift, high common mode rejection and high power supply rejection. Typical MAX455 specs are offset voltage of 1 or 2 mV; offset input drift of 15 to 20 $\mu\text{V}/^\circ\text{C}$; CMRR of 80 dB; power supply rejection of 66 dB at low frequencies and 20 dB at 4 MHz.

The amplifier is unity-gain stable when driving a 75- Ω load (± 1 V maximum). With a gain of +6 dB, it is stable with 150 Ω (± 2 V max), and at a gain of +20 dB, it is stable at 1-k Ω load. The gain-bandwidth increases with load resistance (Fig. 1). The gain also drops with increasing temperature (Fig. 2).

Unlike many fast video amplifiers, it is simple to get unity-gain stability even on a breadboard without using a ground plane. Ground planes are still recommended, since anyone who has ever worked with high-speed amplifiers knows the frustration of trying to stabilize them. Just bypass the MAX455 chip's supplies with 0.1 μF ceramic capacitors to ground and keep all leads short.

OPTIMIZING THE MULTIPLEXER

The chip is also much more stable than a bipolar amplifier when driving a high-capacity load typical of many flash converters. With loads greater than 100 pF, however, a series R should be inserted serially at the output such that the RC product is 10 ns or more at unity gain.

The MAX455 loads the video cable far less than would a separate multiplexer-op amp combination since the multiplexer-out/amplifier is an internal node deliberately not brought out to a bonding path to keep parasitics to a minimum. This allows smaller switches, compared with those in a separate multiplexer, which keeps the channel input capacitance down to about 7 pF on and 3.5 pF off. The multiplexer switch areas were also held to a near-circular shape to minimize the ratio of on-resistance to capacitance.

The multiplexer-out/amplifier-in RC rolloff was held to 80 MHz—about equal to the uni-

ty-gain amplifier bandpass—so the combination gives a typical 50-MHz bandpass for unity gain driving 75 Ω . Input voltage protection was not sacrificed to get the low input capacitance. The inputs have electrostatic discharge protection to greater than ± 2000 V, and a fault current of 100 mA or more is needed to cause SCR latch-up.

The MAX455 multiplexer section uses "T" switches to attain high off isolation and interchannel isolation, typically 70 dB at 4 MHz. This high isolation can only be preserved with careful external wiring. A groundplane should be used, and all unused pins, which provide internal interchannel shielding, should be connected to it. Only channels two and three are physically close and a ground trace should therefore be run between them to cut external crosstalk.

TV SPECS

The multiplexer-amplifier can be used for both visual (TV) and instrument (flash converter) switching. For picture work, like switching teleconferencing or broadcast studio cameras, what's critical is differential gain and phase shift. This is measured as change in a small (0.28 V, 3.58 MHz) signal on a large, slowly varying, 0.7-V ramp. Change in gain means change in contrast over the picture, and change in phase corresponds to a change in color. Ideal specifications would be a phase shift of 0.1° and a gain change of 0.1%. No color or contrast changes would then be noticeable even in a long chain of multiplexers for switching cameras, attenuators, mixers, and so on.

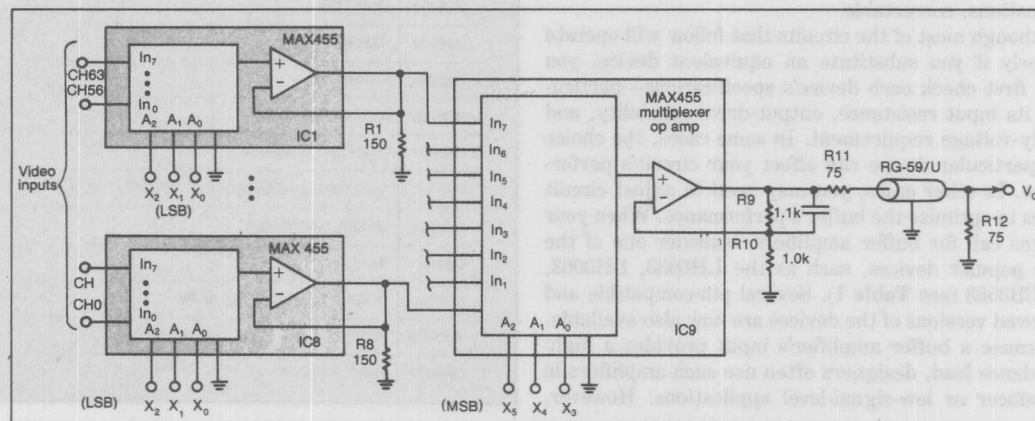
The MAX452 video amplifier (the MAX455 without multiplexer) has a phase error of twice this, or 0.2°, while the MUX455 with eight-channel multiplexer has a phase error of about 1.2°. (The present design optimized bandpass somewhat at the expense of phase linearity.) The

gain error is about 0.5% with or without the multiplexer. Both errors are tolerable though when only a few multiplexer/amplifiers are used in series, such as for small studios, teleconferencing, and remote surveillance. To do better even with a bipolar op amp of several hundred megahertz gain-bandpass may require special multiplexers such as reed relays, which are being phased out, or p-i-n diodes, which take a lot of power.

A typical link in the picture chain might be an amplifier-attenuator for setting the video level for the best signal-to-noise ratio. This could be done in inconvenient binary increments with a digital-to-analog converter, but it is easily accomplished in one decibel step changes with a single MAX455 multiplexer op amp (Fig. 3).

If more than eight multiplexer channels are needed, MAX455s can easily be cascaded with no special precautions other than adding 150 Ω to ground at the first stage output to insure stability (Fig. 4). There is a roll off in the second stage. R9 is 1.1 k Ω to compensate for the 1.5% gain loss of IC1 through IC8. □

Greg Schaffer is a senior member of the technical staff at MAXIM. He has a BSEE from the Massachusetts Institute of Technology, an MSEE from the University of California, Berkeley, and an MS in computer science from the University of Arizona. One of his two patents, a switching amplifier for noise reduction, resulted in a CMOS a-d converter with a resolution of 1 μ V per count.



4. A 64-channel multiplexer can be built by using eight MAX455s to select 8 of the 64 channels and a final MAX455 chip to select each multiplexer. The first stage is operated at unity gain and 150- Ω load, which supplies some 40 MHz peaking to the high-frequency rolloff of the second stage. The -3 dB frequency is typically 35 MHz.

High-speed buffers help solve problems in circuit applications

Although high-speed, unity-gain buffer amplifiers have been available for several years, recent versions serve a wider variety of applications. The high speed of today's devices makes them attractive for use in S/H circuits, active filters, and video switches.

Bob Underwood, *Maxim Integrated Products*

Modern high-speed buffer amplifiers solve a variety of circuit problems, but the design tradeoffs that increase their speed can also degrade their dc performance. Fortunately, these effects are predictable and, in most applications, correctable.

Although most of the circuits that follow will operate properly if you substitute an equivalent device, you must first check each device's specifications—particularly its input resistance, output-drive capability, and supply-voltage requirement. In some cases, the choice of a particular device can affect your circuit's performance. In other cases, you may need to adjust circuit values to optimize the buffer's performance. When your designs call for buffer amplifiers, consider one of the more popular devices, such as the LH0033, LH0063, and BB3553 (see **Table 1**). Several pin-compatible and improved versions of the devices are now also available.

Because a buffer amplifier's input provides a high-impedance load, designers often use such amplifiers in transducer or low-signal-level applications. However,

the buffer amplifier isn't a lightweight contender. Its output can drive a moderate to heavy load. If a buffer amplifier's input is dc coupled to a transducer or other signal source, then the buffer's input impedance is simply its resistance and capacitance as specified in its data sheet. Note, though, that the relationship between input bias current and input voltage is nonlinear in many buffers. So, you must make certain that the input-resistance values for a particular buffer amplifier are specified over the input-voltage ranges you'll use for it.

Several common situations require ac coupling at the

TABLE 1—REPRESENTATIVE BUFFER AMPLIFIERS

TYPE	MANUFACTURERS
BB3553	BURR-BROWN, MAXIM
EL2003	ELANTEC
HA5002	HARRIS
HA5033	HARRIS
HOS100	ANALOG DEVICES
LH0002	ELANTEC, NATIONAL
LH0033	ANALOG DEVICES, ELANTEC, MAXIM, NATIONAL
LH0063	MAXIM, NATIONAL
LM110	NATIONAL
LT1010	LINEAR TECHNOLOGY CORP
MAX460	MAXIM
OPA633	BURR-BROWN

Buffer amplifiers provide high input impedance and drive a moderate to heavy output load.

buffer's input: Such coupling is necessary when you operate the buffer from a single power supply, when you remove a dc level from the signal, and when you use transducers that don't furnish a dc signal. In these applications, you must connect a resistor between a dc supply and the buffer's input to supply the buffer's bias current. The resistor's value must be low enough to supply the buffer's input current without causing too much voltage drop. However, the resistor's value must also be high enough so that it doesn't load the transducer excessively. In either event, the dc-bias resistor usually dominates the buffer circuit's input resistance. Remember that when a transducer supplies a capacitive output, the buffer amplifier's input resistance limits the low-frequency response of the circuit.

A typical bootstrap circuit (Fig 1) provides an input impedance that exceeds the impedance of any of the circuit components. Although the MAX460 buffer operates from a single supply in this circuit, you can reconfigure the circuit to operate with conventional split power supplies. During operation, an ac signal passes through the input capacitor, appears at the input to the buffer, and is available at the buffer's output at nearly unity gain. The output signal is capacitively coupled back to the low end of the input resistor network, which results in an effective multiplication of the resistive value. The circuit's total input capacitance arises from several sources; the intrinsic buffer-input capacitance, stray capacitances within the circuit layout, and the dc bias resistor's capacitance. You can reduce all of these capacitances by judiciously using shields and guards.

The circuit of Fig 1 was tested while operating from a

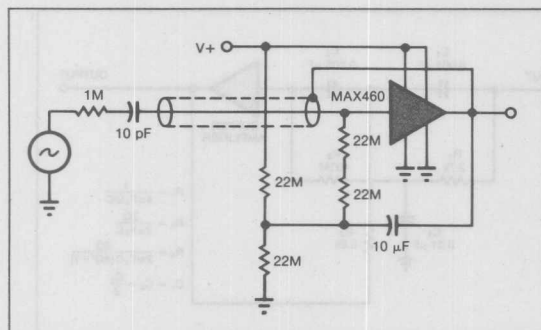


Fig 1—This basic buffer circuit employs bootstrapping techniques that provide an ultrahigh-impedance input for a transducer signal. The MAX460 buffer amplifier operates from a single power supply, but you can reconfigure the circuit to operate from a dual supply.

source resistance of 1 M Ω in series with a 10-pF capacitor. Under these conditions, the measured low-frequency -3 -dB point was 3.3 Hz, and the low-frequency input circuit's time constant was 48 msec. These values are equivalent to those you would measure for a 4800-M Ω shunt-input resistor and a 10-pF series capacitor. The high-frequency input time constant was 0.7 μ sec and had a -3 -dB point of 227 kHz, which equates to an input capacitance of 0.7 pF when you use the 1-M Ω series resistor. An input capacitance this small might be difficult to reproduce because it depends greatly on the configuration of the driven guards connected to the output. Also, the buffer amplifier's case was connected to the output, and the test circuit had no special mechanical support for the input node. However, it should be possible to obtain a 1- or 2-pF input capacitance by connecting guards to the output and by supplying Teflon standoffs for mechanical support.

Buffer amplifiers can also serve in sample-and-hold (S/H) amplifier applications. In most such circuits, you need a buffer amplifier so that the output load does not discharge the hold capacitor (Fig 2). You can consider almost any of the available buffer amplifiers for this application, but in terms of low input current, some are better than others. For example, the MAX460 was designed for this type of application; its input current is low and is virtually independent of the input voltage.

In an S/H application, the switch's characteristics are critical. Ideally, the switch should have no offset voltage, low or zero on-resistance, and low or zero leakage, both across its contacts and from its output contact to its control terminal. Any capacitance between the switch's control terminal and its output couples a charge from the control input to the charge-storage capacitor. As a result, switching from the sample mode to the hold mode adds an error voltage to the analog signal being held by the circuit. It's sometimes possible to calibrate an S/H circuit to account for such a constant

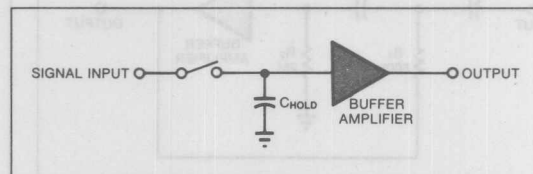


Fig 2—This basic sample-and-hold circuit charges a capacitor by passing an analog signal through a switch. Opening the switch holds the charge on the capacitor. The buffer amplifier's high-impedance input prevents the output load from discharging the capacitor.

The bootstrap technique creates an input impedance value that exceeds the impedance of the individual circuit components.

Because the level-translator circuit is inherently non-saturating, the transistor's storage time is not a critical consideration. In fact, you can use high F_T RF transistors for all four devices. The collector loads of Q_3 and Q_4 are returned to the analog input voltage (buffered by IC_1), which keeps the analog and digital circuits completely balanced. Note that the circuit also provides a set of dummy switches. The circuit's balanced nature is the secret of its excellent hold-step performance. The measured charge injection of the circuit in breadboard fashion—and without any circuit adjustments—was 100 mV into a 33-pF hold capacitor, which represents a 0.165 pJ charge injection. A stray capacitance of 1 pF between the FET switch's gate and the hold capacitor would just about account for such a small hold step.

The breadboarded circuit was adjusted, with a short piece of stiff wire, to add about 1 pF of capacitance between the compensating gate and the hold capacitor. By moving the wire, you can adjust the circuit to put out 0V for a 0V analog input. When properly adjusted, the circuit gave an output error of only a few millivolts over the S/H circuit's entire $\pm 10V$ analog-input range. Also, replacing any of the semiconductor components had no effect on the hold step. In short, you don't need closely matched components for this type of S/H circuit.

Construct active filters, too

You can also use buffer amplifiers to build filters of various configurations. Although lowpass filters and other filter types do have their uses, notch and highpass filters have the most practical applications. For example, you can use a 2-pole highpass filter to remove low-frequency signal components with little effect on signals that occur above the filter's cutoff frequency. As Fig 4 shows, the basic filter circuit exhibits a damping factor of 1 and a cutoff frequency of 1 kHz. The damping

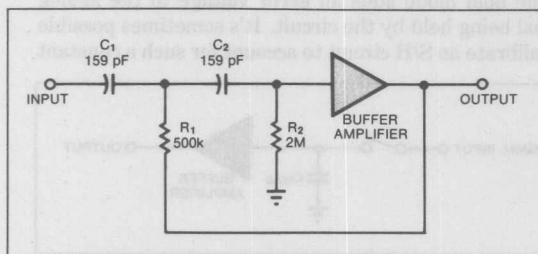


Fig 4—This basic 2-pole, highpass filter requires only a buffer amplifier and a few passive components. This circuit has a cutoff frequency of 1 kHz and a damping factor of one. The damping factor is set by the ratio of R_1 to R_2 .

factor is controlled by the ratio of R_1 to R_2 . You can scale the filter's frequency by changing the capacitor values, but both values must be equal.

Often referred to as a bridged-tee notch filter, the circuit shown in Fig 5 consists of a series resistance and a shunt capacitance, bridged by a series-capacitance and a shunt-resistance section. In this filter circuit, dc levels pass through the series resistors, while at frequencies well above the notch the resistors have no effect. Instead, the high-frequency signals pass through the series capacitors and go on through the buffer to the output. Only the accuracy of the components, the loading by the output buffer amplifier, and any stray capacitance incurred in the filter's construction limit the maximum signal rejection at the notch frequency.

The readily available component values shown in Fig 5 create a notch filter centered at 60 Hz. If you use 1%-tolerance resistors and 2.5%-tolerance capacitors, adjust the notch by trimming R_3 for a null at 60 Hz. When properly adjusted, the notch is deeper than -60 dB at 60 Hz, and the notch width is about 2.5 Hz at -40 dB.

Filters aren't the only signal-processing application for buffer amplifiers. You can use buffer amplifiers in video-signal switches, too. For example, an IH5352 chip lets you construct a moderate-performance 2-input, 2-output video crosspoint switch. But because the IH5352 has high shunt capacitance and high series resistance, problems can arise when you use the chip directly in high-performance video circuits. Luckily, you can alleviate the problems by buffering the video switch's input and output signals.

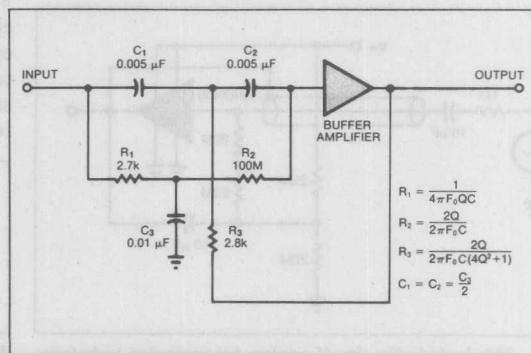


Fig 5—This bridged-tee notch filter produces a -60 dB notch at 60 Hz. The buffer amplifier provides the necessary high input impedance.

error, but often the charge injection is not constant; it varies with input voltage, temperature, or time. Thus, it's best to minimize any charge-injection errors by minimizing the switch's parasitic capacitances.

The SD5000 DMOS switch IC is a good choice for S/H applications: When the chip's switch is closed, it has no offset voltage. The switch's capacitances are reasonably low, and it offers tolerably low on-resistance and leakage current. Because the SD5000 device provides four independent switches, you can connect two switches in parallel to further lower the circuit's on-resistance. You can also use the two remaining switches as a dummy capacitor, which lets you balance any charge that might be injected by the active switch section. Such a technique can result in nearly a tenfold reduction in the injected charge, without any need for manual circuit adjustments. However, if you require even better performance, you can add manually adjustable components to the circuit.

The hold capacitor is the heart of all S/H circuits. As such, it must have a high breakdown voltage and low leakage current, and it should be made of a material that has a low dielectric absorption. Typically, polycarbonate, polystyrene, and polypropylene exhibit good dielectric characteristics, but glass, mica, and most ceramics do not.

Some S/H circuits—particularly those that employ low-charge-injection techniques—may require only a switch, a hold capacitor, and an output buffer. More often, however, the circuit demands an input buffer amplifier, too. Without an input amplifier, the signal source must supply the hold capacitor's charging current.

Build high-speed S/H circuits

A realistic S/H circuit (Fig 3) contains an input buffer amplifier (IC₁), an output buffer amplifier (IC₂), and a DMOS FET switch. A voltage-level translator circuit made up of transistors Q₁ through Q₄ converts the ECL-compatible input signals to a voltage (referenced to the analog signal voltage) that drives the DMOS FET switches. The circuit employs Q₁ and Q₂ to form a differential amplifier that accommodates the balanced incoming ECL signals (Q and $\bar{Q}$). The four transistors are high-speed types that have a gain-bandwidth product (F τ) in the gigahertz range. Transistors Q₁ and Q₂ must have a breakdown-voltage rating that at least equals the circuit's positive supply voltage plus the ECL common-mode voltage of -2V. In this circuit, a breakdown-voltage rating of 17V is adequate. Likewise, transistors Q₃ and Q₄ require breakdown voltages of at least 25V to allow for a -10V analog input.

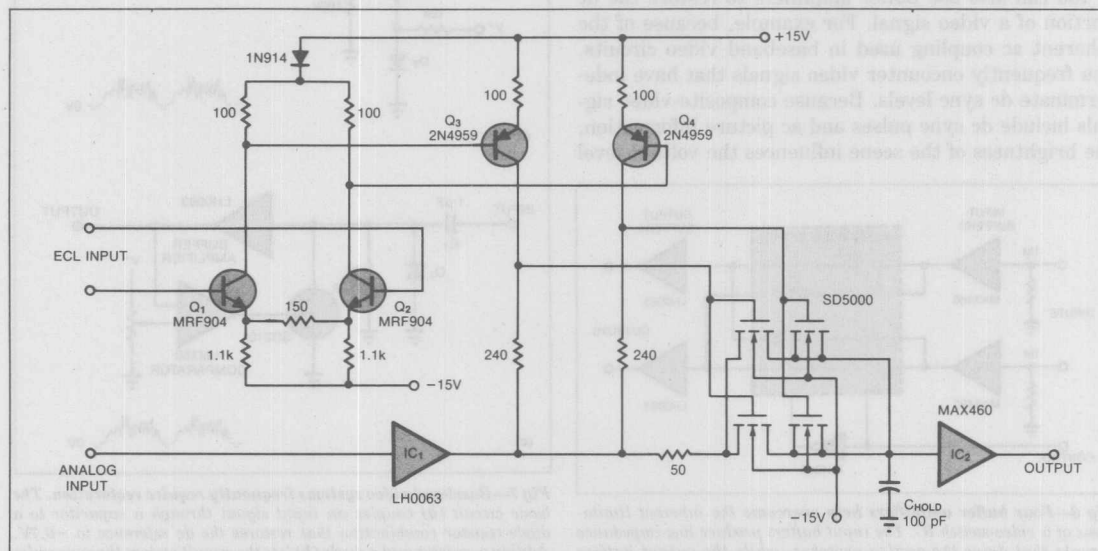


Fig 3—This high-speed S/H circuit includes an input buffer, a DMOS switch, and an output buffer. High-frequency transistors Q₁, Q₂, Q₃, and Q₄ form a level translator that converts the ECL input signal into a voltage that can drive the switch's gates.

In the circuit shown in Fig 6, the two video inputs feed through input buffer amplifiers (IC₁ and IC₂) to generate low-impedance signals that drive the analog-switch IC. Depending upon the input signal's source, each buffer-amplifier input may require a termination resistor. The termination resistors keep the amplifiers from saturating if an input is unconnected or is fed with an ac-coupled signal. A disconnected channel, for example, could turn on the switches and feed a high dc voltage to the output buffers. Because of the buffer amplifiers' input capacitances, a slight impedance mismatch may exist at the input terminals, but it usually doesn't limit the circuit's performance.

If you can accept a 6-dB loss through the switches, you can eliminate the output buffer amplifiers (IC₃ and IC₄). Such a loss might be tolerable, but switch-resistance values can vary considerably, which leads to an uncertainty about the actual signal loss. The output buffer amplifiers solve the loss-uncertainty problem and at the same time provide a low-impedance output that drives transmission lines either directly or through an accurate termination resistor. When operating from a $\pm 15\text{V}$ power supply, the video circuit (Fig 6) handles a $\pm 10\text{V}$ signal.

Restore dc levels

You can also use buffer amplifiers to restore the dc portion of a video signal. For example, because of the inherent ac coupling used in baseband video circuits, you frequently encounter video signals that have indeterminate dc sync levels. Because composite-video signals include dc sync pulses and ac picture information, the brightness of the scene influences the voltage level

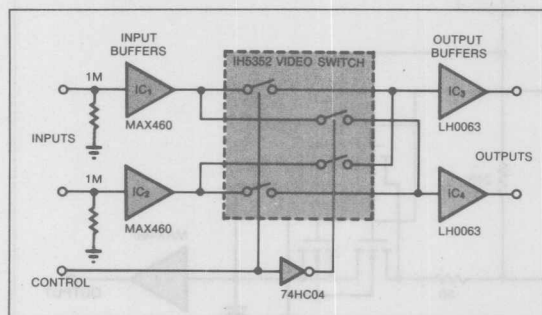


Fig 6—Four buffer amplifiers help overcome the inherent limitations of a video-switch IC. The input buffers produce low-impedance signals that drive the analog switches, while the output buffers eliminate gain variations that result from unmatched switch resistances.

of the sync pulses as the complete video signal passes through an ac-coupled circuit. You can use several methods to re-reference the signal to ground.

The classic dc-restorer circuit (Fig 7a) passes the ac input signal through a capacitor (C_1) to a diode-resistor shunt (D_1 - R_1). The time constant for R_1 and C_1 must be long enough to pass the lowest frequency component of interest in the input waveform, yet short enough to recover quickly from a fast change in the input waveform. However, the diode's forward-voltage drop produces a signal that is dc-restored to -0.7V , not to ground. By adding a resistor and an additional diode (Fig 7b) you can restore the video signal's sync pulse to

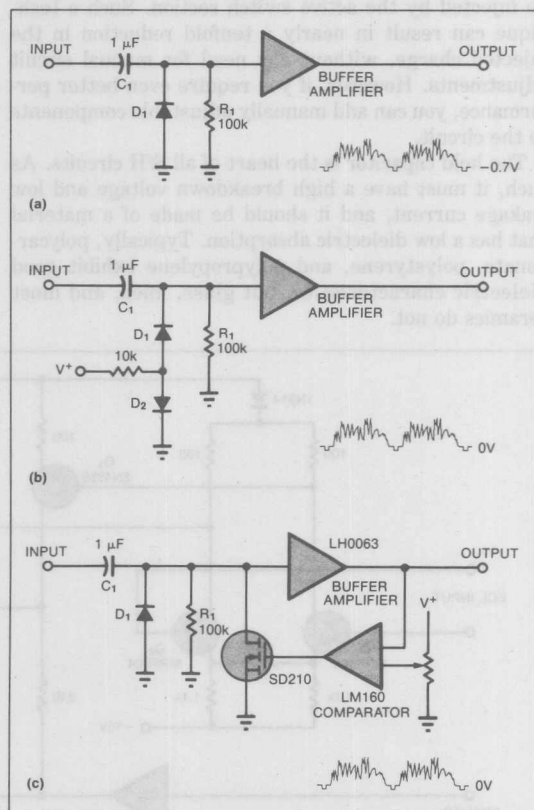


Fig 7—Baseband video systems frequently require restoration. The basic circuit (a) couples an input signal through a capacitor to a diode-resistor combination that restores the dc reference to -0.7V . Adding a resistor and a diode (b) lets the circuit restore the sync pulse to 0V . You can further refine the circuit by adding an analog switch and a comparator (c).

0V. The added diode (D_2) produces a 0.7V output that should exactly cancel the forward voltage of D_1 . The added diode also cancels D_1 's $-2 \text{ mV}/^\circ\text{C}$ temperature coefficient. In practice, the current in D_1 depends on the input signal's characteristics, so an exact cancellation of forward-voltage drops and temperature coefficients is difficult to achieve. You won't be able to match the diodes' voltages to better than several tens of millivolts. The circuits shown are suitable for positive signals, but they can process negative-going signals if you reverse the polarity of the diodes.

A more sophisticated approach (Fig 7c) requires you to add an analog switch and a comparator to the basic dc-restoration circuit. In the new circuit, you bias the comparator a few hundred millivolts above ground so that the comparator recovers the composite sync information, rejects the video part of the signal, and turns on the SD210 analog switch during sync time. The comparator's action puts a voltage on C_1 that equals the input signal's voltage during the previous sync pulse. In effect, the circuit subtracts the stored charge from the incoming waveform, which yields a 0V signal during the sync interval. Diode D_1 speeds the recovery from any fast change in the input signal's dc level. Without the diode, the comparator might force the analog switch to conduct during the complete video cycle or at least until R_1 could act to bring the buffer amplifier's input voltage back into range.

EDN

Author's biography

Bob Underwood is a senior member of the technical staff for hybrid design at Maxim (Sunnyvale, CA); he has been with the company for four years. Prior to joining Maxim, he was employed by National Semiconductor. Bob has a BSEE and an MSEE from Washington University in St Louis, MO, and he is a member of the International Society for Hybrid Microelectronics (ISHM) and the American Radio Relay League (ARRL). In his spare time Bob enjoys classical music, photography, and amateur radio, in which he holds an Extra-class license.

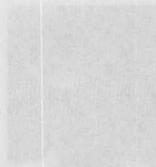


EDN January 21, 1988

the most signal's characteristics, as an exact calculation of forward voltage drops and temperature coefficients is difficult to achieve. You won't be able to match the diodes' voltages to better than several tenths of millivolts. The circuit shown was suitable for positive signals, but they can process negative-going signals if you reverse the polarity of the diodes.

A more sophisticated approach (Fig. 7c) requires you to add an analog switch and a comparator to the basic de-rectifier circuit. In the new circuit, you bias the comparator a few hundred millivolts above ground so that the comparator reverses the constant zero level. When the signal is at the zero level, the comparator's output goes to a voltage on C1 that equals the input signal's voltage during the previous zero pulse. In effect, the circuit subtracts the stored charge from the incoming waveform, which yields a 0V signal during the zero interval. Diode D1 speeds the recovery from any last charge in the input signal's diode. Without the diode, the comparator might force the analog switch to conduct during the complete video cycle or at least until it could not to bring the buffer amplifier's input voltage back into range.

Author's biography



Bob Labovitz is a senior member of the technical staff for light design at Shure. He has been with the company for over 20 years. He has a B.S. in Electrical Engineering from the University of Illinois at Chicago. He has been a member of the International Society for Optical Engineering (ISPE) and the American Radio Relay League (ARRL) for the past 10 years. He has been a member of the International Society for Optical Engineering (ISPE) and the American Radio Relay League (ARRL) for the past 10 years. He has been a member of the International Society for Optical Engineering (ISPE) and the American Radio Relay League (ARRL) for the past 10 years.

Interface (RS-232), Display Drivers, Timers, Counters

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Interface (RS-232), Display Drivers, Timers, Counters

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Although the RS-232 specification recommends that the maximum cable length should be less than 15 meters, much longer cable lengths are fairly common. A problem sometimes encountered, particularly when using long cables, is that ground potential differences between the two ends of the cable can be higher than the 2V noise margin built into the RS-232 specification. Another possibility that must sometimes be considered is the potentially disastrous effects of accidental connection of the RS-232 inputs or outputs to high voltages such as the 110/220VAC power line. Opto-isolation both isolates the computer or instrument from possibly harmful voltages and allows operation with a large voltage difference between the grounds at each of an RS-232 link.

The MAX635 DC-DC converter IC provides an isolated power supply by regulating the output of the transformer primary. With a bifilar wound (1 to 1 turns ratio) transformer, when the output of the primary is regulated to 5V, the output of the secondary will be semi-regulated to 5V. Line and load regulation is easily kept to $\pm 10\%$ if the primary and secondary are tightly coupled by using bifilar winding techniques. The data is transferred via the two 4N26 optocouplers.

Three new Maxim Isolated RS-232 devices: MAX250, MAX251, and MAX252 incorporate built in isolation for even fewer external components.

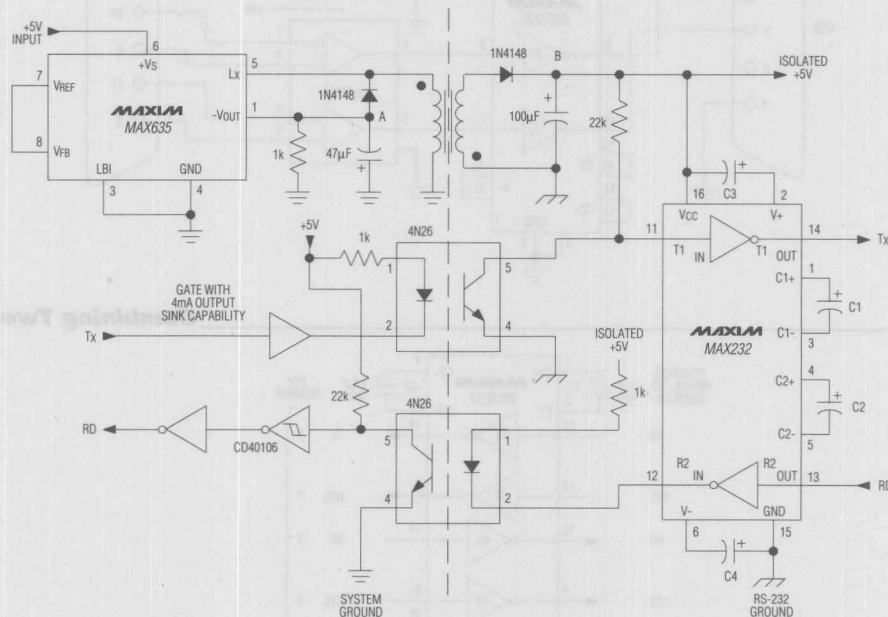


Figure 6-1.

Although most terminals, computers, and printers use the RS-232 (CCITT V.24) standard for their serial communication port, some equipment uses the RS-422 or RS-485 balanced or differential standard to achieve a higher data rate, or to accommodate up to $\pm 5V$ voltage difference between the ground potentials between the two pieces of equipment which communicate via RS-422. This

circuit, which uses only a single +5V supply, accepts RS-232 inputs and converts them to RS-422 outputs. In the other direction, it accepts RS-422 inputs and converts them to RS-232 outputs. The MAX233 converts the +5V power supply input to $\pm 9V$, using 4 internal capacitors.

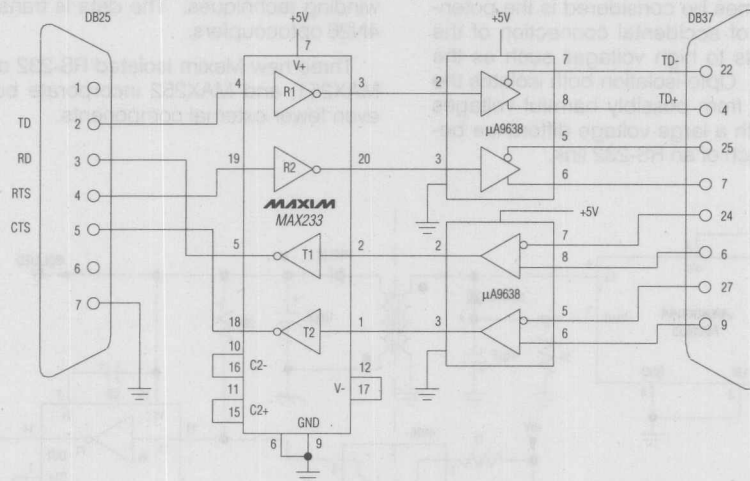


Figure 6-2.

Combining Two MAX232s

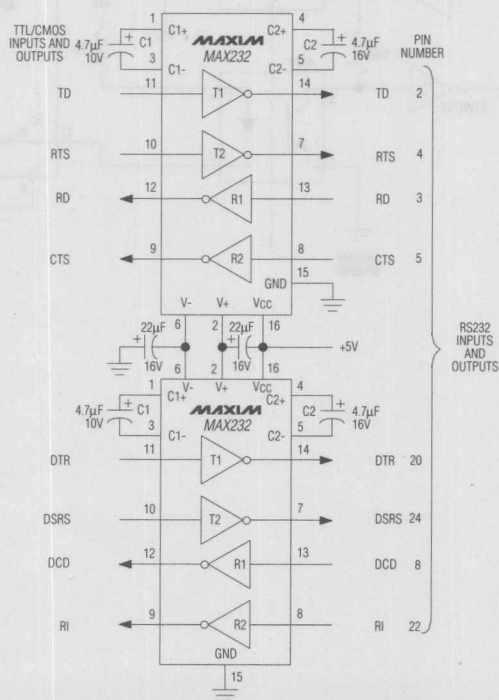


Figure 6-3.

Connecting a diode in series with the V+ power input of the MAX231 and MAX239 allows power supply sequencing at V+ and VCC to be ignored. If no diode is present, the 12V V+ supply must rise to 5V before VCC reaches 5V. In most systems supply sequencing is correct, and no diode is needed, if power is applied to both supplies at the same time. If this is not the case, or if sequencing is uncertain, the diode connection is recommended. This will replace the standard circuit for these devices in all future literature.

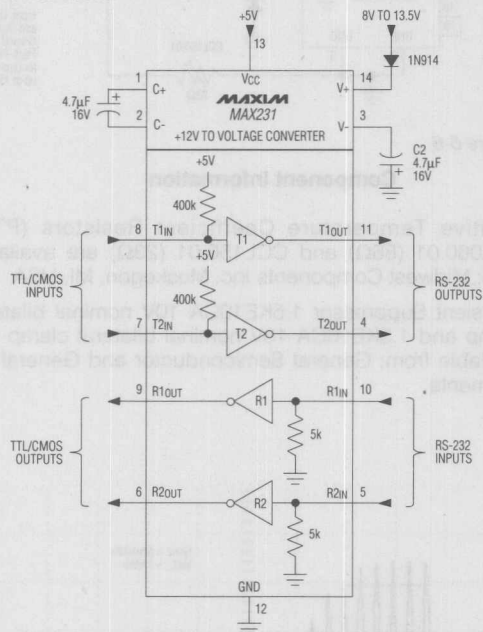


Figure 6-4.

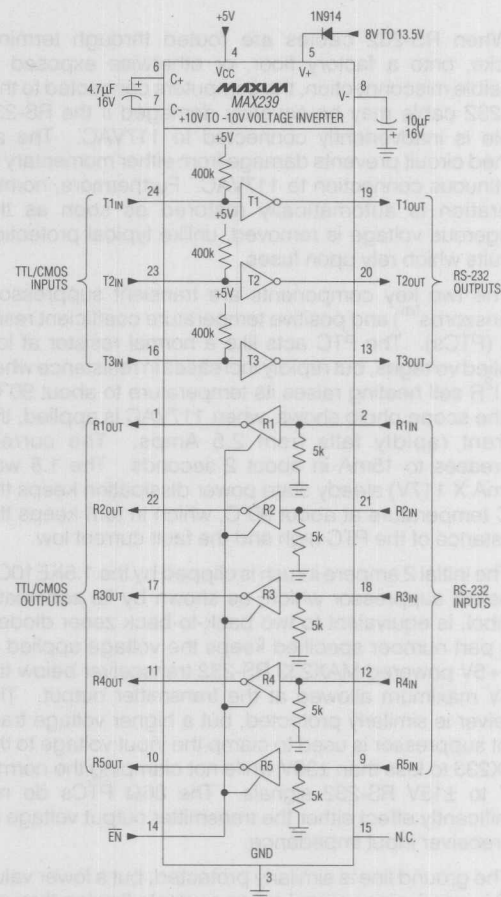


Figure 6-5.

When RS-232 cables are routed through terminal blocks, onto a factory floor, or otherwise exposed to possible misconnection, the computers connected to that RS-232 cable may be severely damaged if the RS-232 cable is inadvertently connected to 117VAC. The attached circuit prevents damage from either momentary or continuous connection to 117VAC. Furthermore, normal operation is automatically restored as soon as the dangerous voltage is removed, unlike typical protection circuits which rely upon fuses.

The two key components are transient suppressors (Transzorb[™]) and positive temperature coefficient resistors (PTCs). The PTC acts like a normal resistor at low applied voltages, but rapidly increases in resistance when the I^2R self heating raises its temperature to about 90°C. As the scope photo shows, when 117VAC is applied, the current rapidly falls from 2.5 Amps. The current decreases to 15mA in about 2 seconds. The 1.8 watt (15mA X 117V) steady state power dissipation keeps the PTC temperature at about 90°C, which in turn keeps the resistance of the PTC high and the fault current low.

The initial 2 ampere inrush is clipped by the 1.5KE10CA transient suppressor which, as shown by its schematic symbol, is equivalent to two back-to-back zener diodes. The part number specified keeps the voltage applied to the +5V powered MAX233 RS-232 transceiver below the ±15V maximum allowed at the transmitter output. The receiver is similarly protected, but a higher voltage transient suppressor is used to clamp the input voltage to the MAX233 to less than ±30V while not clamping the normal ±5V to ±15V RS-232 signals. The 86Ω PTCs do not significantly effect either the transmitter output voltage or the receiver input impedance.

The ground line is similarly protected, but a lower value PTC is used, since signal return currents flowing through the PTC in the ground lead will cause a voltage difference in ground potential between the two ends of the RS-232 cable, thereby changing the apparent voltage levels at the RS-232 inputs. The MAX233 input receivers are specified with V_{IL}/V_{IH} of 0.8V and 2.4V, which are well within the RS-232 limits of -3V and +3V, so the system still fully complies with RS-232 specifications with up to 600mV of voltage drop across the PTC in the ground lead. Under normal operation the signal return current will never be more than 5mA per RS-232 line (15V max output V ÷ 3kΩ minimum receiver input impedance), so the drop across the PTC in the ground line is less than 250mV.

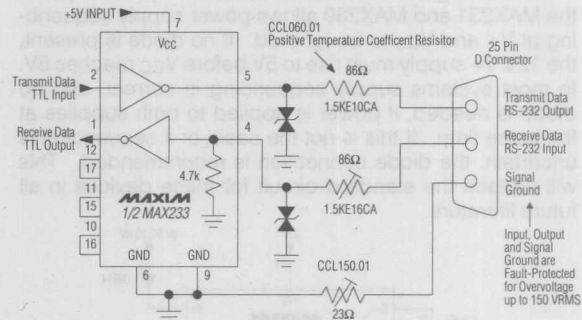


Figure 6-6.

Component Information

Positive Temperature Coefficient Resistors (PTC) CCL060.01 (86Ω) and CCL150.01 (23Ω) are available from: Midwest Components Inc. Muskegon, MI, USA

Transient Suppressor 1.5KE10CA 10V nominal bilateral clamp and 1.5KE16CA 16V nominal bilateral clamp are available from: General Semiconductor and General Instruments

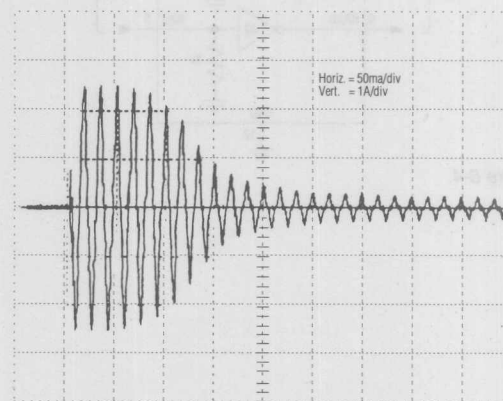


Figure 6-7. Input Current After Application of 110VAC to RS-232 Transmit or Receive Line

Table 6-1. Circuit Definitions/Pin Assignments for RS-232/V.24

PIN	EIA RS-232 CIRCUIT	CCITT V.24 CIRCUIT	DESCRIPTION	TYPE	SOURCE
1	AA	101	Protective Ground	Ground	Ground
2	BA	103	Transmitted Data	Data	DTE
3	BB	104	Received Data	Data	DCE
4	CA	105	Request To Send	Control	DTE
5	CB	106	Clear To Send	Control	DCE
6	CC	107	Data Set Ready	Control	DCE
7	AB	102	Signal Ground/Return	Ground	Ground
8	CF	109	Received Line Signal Detector	Control	DCE
9	-	-	Reserved for Data Set	Testing	
10	-	-	Reserved for Data Set	Testing	
11	-	-	Unassigned		
12	SCF	122	Sec. Received Line Signal Detector	Control	DCE
13	SCB	121	Secondary CTS	Control	DCE
14	SBA	118	Sec. Transmitted Data	Data	DTE
15	DB	114	Transmission Signal Element Timing (DCE)	Timing	DCE
16	SBB	119	Sec. Received Data	Data	DCE
17	DD	115	Receiver Signal Element Timing (DCE)	Timing	DCE
18	-	-	Unassigned		
19	SCA	120	Secondary RTS	Control	DTE
20	CD	108.2	Data Terminal Ready	Control	DTE
21	CG	110	Signal Quality Det.	Control	DCE
22	CE	125	Ring Indicator	Control	DCE
23	CH/CI	111/112	Data Signal Rate Selector (DCE/DTE)	Control	DTE/DCE
24	DA	113	Transmit Signal Element Timing (DTE)	Timing	DTE
25	-	-	Unassigned		

Table 6-2. Circuits Commonly Used for RS-232 and V.24 Asynchronous Interfaces

PIN	CIRCUIT	DESCRIPTION
1	Protective Ground	Connect to Earth Ground
2	Transmit Data (TD)	Data from DTE
3	Receive Data (RD)	Data from DCE
4	Request To Send (RTS)	Handshake from DTE
5	Clear To Send (CTS)	Handshake from DCE
6	Data Set Ready (DSR)	Handshake from DCE
7	Signal Ground	Reference Point for Signals
8	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
11	Printer Busy Signal	Handshake from Printer
20	Data Terminal Ready	Handshake from DTE
22	Ring Indicator	Handshake from DCE

Table 6-3. Summary of RS-232 and V.28 Electrical Specifications

PARAMETER	SPECIFICATION	COMMENTS
Driver Output Voltage		
0 level	+5V to +15V	With 3-7k Ω load
1 level	-5V to -15V	With 3-7k Ω load
Max. output	± 25 V Max.	No Load
Receiver Input Thresholds (data and clock signals)		
0 level	+3V to +25V	
1 level	-3V to -25V	
Receiver Thresholds		
RTS, DSR, DTR		
On level	+3V to +25V	
Off level	Open Circuit or 3V to -25V	Detects Power Off Condition at Driver
Receiver Input Resistance	3k Ω to 7k Ω	
Driver Output Resistance		
Power off condition	300 Ω Min.	$V_{OUT} < \pm 2$ V
Driver Slew Rate	30V/ μ s Max.	3k $\Omega < R_L < 7$ k Ω ; 0pF < $C_L < 2500$ pF
Signalling Rate	Up to 20k bits/sec.	
Cable Length	50'/15m. Recommended Max. Length	Longer cables permissible if $C_{LOAD} \leq 2500$ pF

By modulating the display driver's shutdown input, you can vary the brightness of a multiplexed LED display without affecting the circuit's multiplex action. This approach is useful in panel meters and other instrument applications because it eliminates the need for external buffers or FETs and their associated power losses. A few passive components and an inexpensive timer (IC1) generate the required pulse-width-modulated signal (Fig 6-8).

Diode D1 lets the timer produce duty cycles below 50%. (Without the diode, duty cycles range from 50% to 100%.) D1's presence also separates the charge and discharge paths for timing capacitor C1, thereby enabling potentiometer R2 to vary the output's duty cycle without affecting its frequency. (Or, the microprocessor can control the duty cycle, and hence display brightness, if you replace R1 with a digitally controlled potentiometer such as Xicor's model X9MMEI.)

Frequency remains constant because the sum of the charge and discharge times is constant: Charge time, proportional to the resistance in R1 and the upper portion of R2, corresponds to high portions of the output waveform. Discharge time, proportional to the resistance in the lower portion of R2, corresponds to low portions of the output waveform. The maximum duty cycle is 100%. R1, however, included as a current-limiting resistor for pin 7, limits the minimum duty cycle to 7%.

C1's 4.7nF value provides 5-kHz operation—well within the recommended range of 3 to 9 kHz. Below 2 kHz (the scan rate for individual digits) some digits will remain off. Above 9 kHz, "ghost" digits appear because the interdigit blanking period is too short.

The timer's output signal drives IC2's Shutdown input (pin 10). When low, the signal turns off the internal multiplex-scan oscillator, digit drivers, and segment drivers. This action has no effect on data stored in the chip's 8-byte RAM, or on write operations to that memory.

IC2 operates in one of three modes according to the signal level at pin 9: Driving the pin high causes the chip to decode its data for hexadecimal display. Letting the pin float enables decoding for code B display, and driving the pin low shuts down the chip in a low-power standby mode. The Fig 6-9. circuit is for hex display only. For other applications, you can choose one of the pin-9 drive circuits shown below.

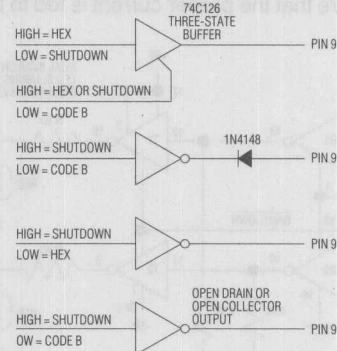


Figure 6-9. Connecting one of these drivers to pin 9 of the display driver lets you command other modes of operation that your application may require.

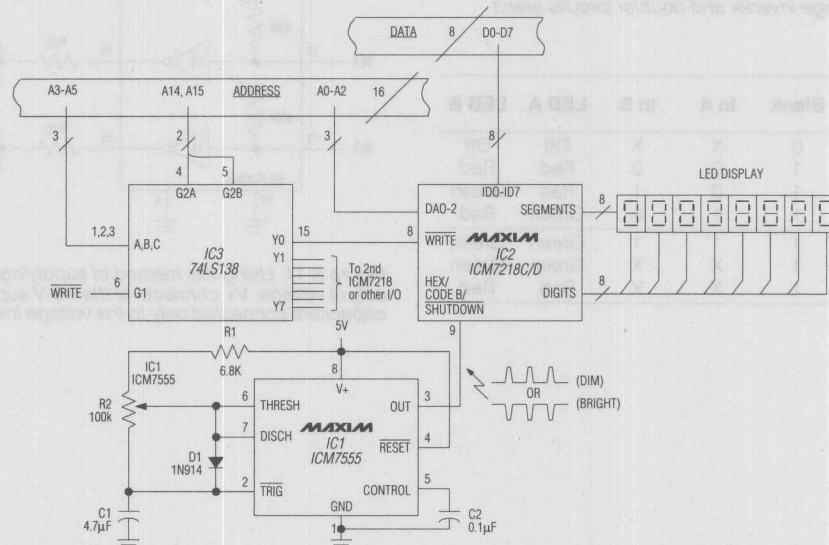


Figure 6-8. Adjusting R2 varies the output duty cycle from timer IC1, which in turn varies the LED brightness. Decoder IC3 allows the host microprocessor to address the display driver (IC2).

A MAX232 RS232 transceiver chip can double as a bicolor light-emitting (LED) driver. It can configure a circuit that uses only one transmitter per bicolor LED and has the ability to blank the display (by turning off the LEDs) and supply a test-mode operation that forces a red or green color to appear on all the LEDs.

Several methods of supplying the driving voltage to the transmitter outputs are available. Using one of the methods, V+ is connected directly to the +5V supply, and the V- terminals are connected to an external -5V supply. Here, the chip's internal voltage inverter and doubler circuits aren't used.

An LED current-limiting resistor, R_{LED} in this case, makes sure that the proper current is fed to the LEDs; the

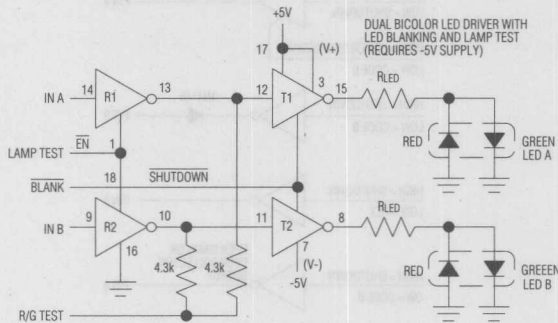


Figure 6-10. In this LED-Driver Circuit, the chip's V+ terminal connects directly to the +5V supply, and the V- terminal connects to an external -5V supply. In this configuration, the chip's internal voltage inverter and doubler circuits aren't being used.

R/G test	Lamp Test	Blank	In A	In B	LED A	LED B
X	X	0	X	X	Off	Off
X	0	1	0	0	Red	Red
X	0	1	0	1	Red	Green
X	0	1	1	0	Green	Red
X	0	1	1	1	Green	Green
0	1	1	X	X	Green	Green
1	1	1	X	X	Red	Red

internal resistance of the circuit's output driver (Tx) is usually sufficient with the 5V supply (Fig. 6-10).

The output voltage can also be supplied to the transmitter outputs when the V+ terminal connects to the +5V supply, with no capacitors connected to the 5 to 10V voltage-doubler circuit (Fig 6-11). In this case however, the +10 to -10V inverter does connect to capacitors C2 and C3. These capacitors invert the voltage signal on pin 9 (V+). Because V+ is merely 5 V, the V voltage will be just -5V from the inverter circuit. Of course, the power-supply arrangements employed in the two circuits can be interchanged without any ill effects.

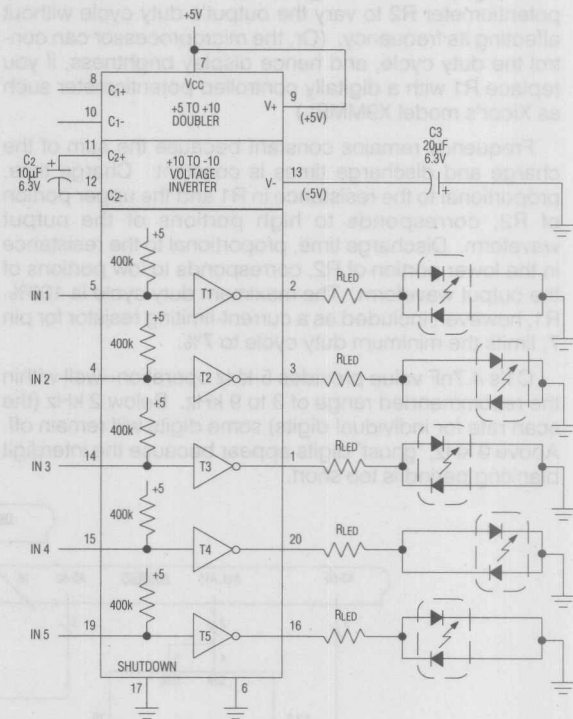


Figure 6-11. Using this method of supplying an LED-driving output voltage, V+ connects to the +5-V supply with capacitors connected only to the voltage inverter circuit.

Four Digit Display Decoder/Drivers

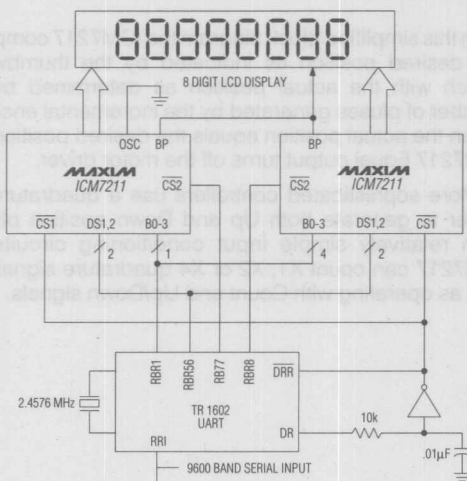


Figure 6-12. Remote LCD Display via UART

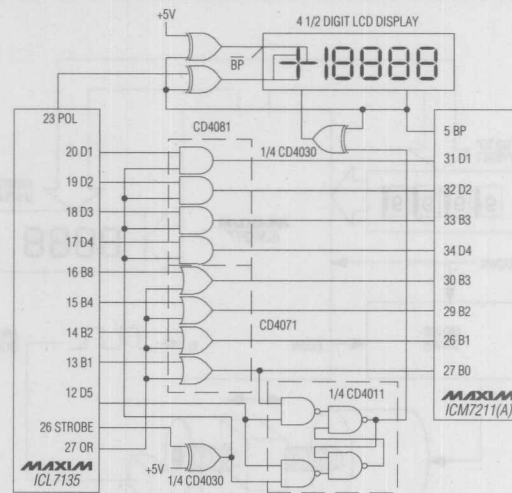


Figure 6-14. LCD Display for ICL7135 A/D

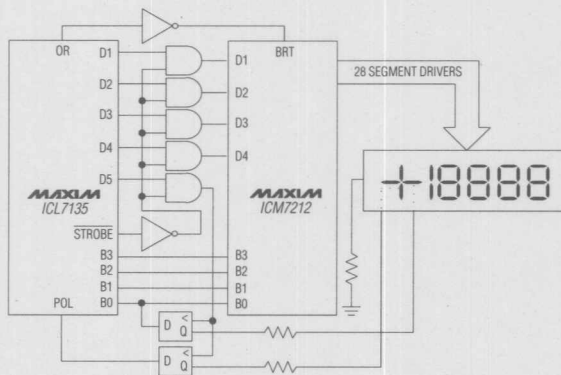


Figure 6-13. LED Display Interface for ICL7135 A/D

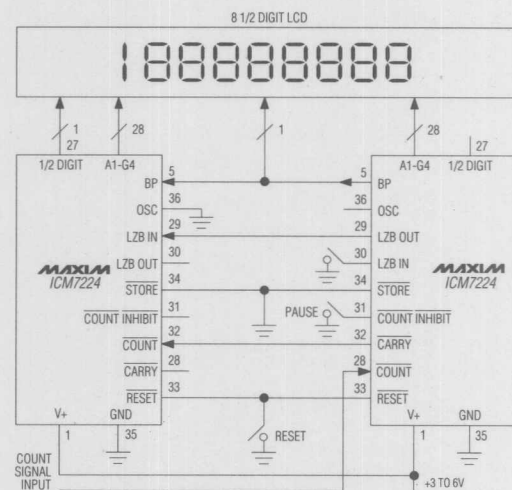


Figure 6-15. 8 1/2 Digit Counter/Totalizer

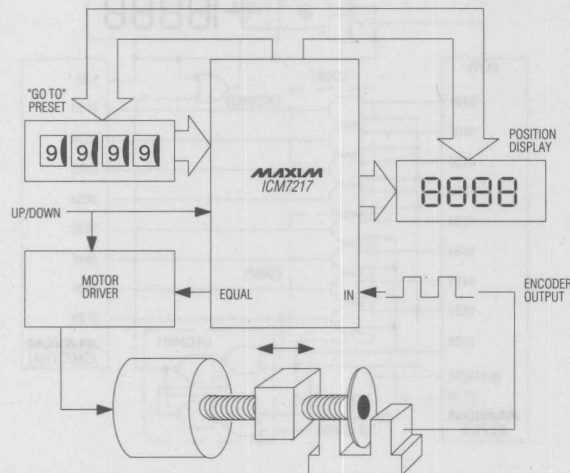


Figure 6-16.

In this simplified block diagram the ICM7217 compares the desired position as indicated by the thumbwheel switch with the actual position as determined by the number of pluses generated by the incremental encoder. When the actual position equals the desired position, the ICM7217 Equal output turns off the motor driver.

More sophisticated controllers use a quadrature encoder to generate both Up and Down position pluses. With relatively simple input conditioning circuits the ICM7217 can count X1, X2 or X4 quadrature signals, as well as operating with Count and Up/Down signals.

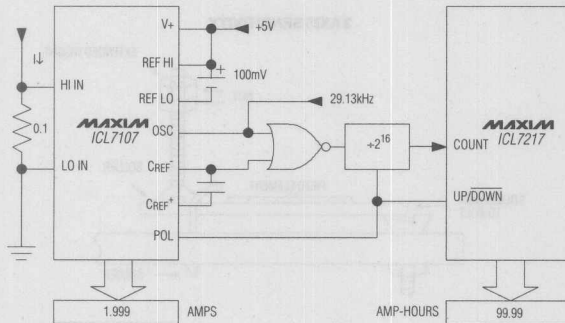
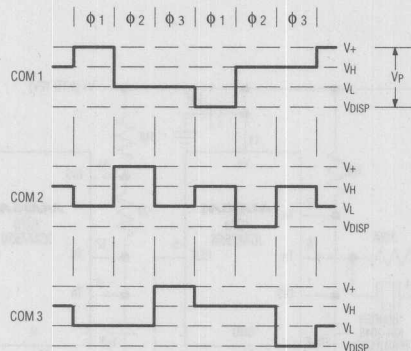


Figure 6-17.

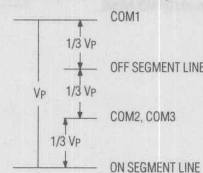
This Amp-Hour meter uses the ICL7107 A/D to both display the instantaneous current, and to generate a stream of pulses which are integrated and displayed by the ICM7217 counter. Thumbwheel presets can be added to the ICM7217 to perform control functions, such as shutting off the power supply in a plating operation or battery charger once the desired AMP-Hour charge has been reached.

The common mode shift of the reference capacitor during the Deintegrate phase is used to generate a pulse stream that is proportional to the oscillator frequency. The ICL7107 scale factor is set by the reference voltage and the 0.1 ohm resistor. The Amp-Hour scale factor can be adjusted by changing either the oscillator frequency or the 2^{16} prescaler.

Triplexed LCD Waveforms



VOLTAGE LEVELS DURING $\phi 1$



OFF SEGMENT
- $1/3 V_p$ TO ALL COMMONS
ON SEGMENT
- V_p TO COM1
- $1/3 V_p$ TO COM2, COM3

Triplexed LCDs have three backplanes, and every segment line drives three separate segments, one for each backplane. The backplane waveforms have 6 separate phases.

During each of the first three phases, one backplane is at the most positive voltage, while the other two are at the lower intermediate voltage, V_L . The remaining three phases are an inversion of the first three: the three backplanes are each connected to the lowest voltage, V_{DISP} , for one phase while the other two backplanes are at the higher intermediate voltage, V_H .

The problem that must be solved is how to turn ON or OFF each of the three segments that are driven by a single segment drive line. To turn ON the segment referenced to COM1 (backplane 1), the LCD display driver will drive the segment drive line to the lowest display voltage. This applies the full display voltage across the segments referenced to COM2 and COM3. This $1/3$ display voltage is below the turn-on threshold of the display, so these segments are not turned ON during this phase.

If the segment referenced to COM1 is supposed to be OFF, the LCD display driver drives the segment line to the upper intermediate voltage level, thereby applying 1.3 display voltage to all three segments driven by the segment line.

Figure 6-18

Piezo-electric resonators have a dual property: they produce an electric field when bent (piezo-electric effect), and they produce physical movement when voltage is applied (electrostrictive motion). Both effects contribute to operation of the circuit in Fig 6-21, which sounds an alarm in response to a jolt, vibration, or other physical movement.

When an applied movement flexes the shock sensor (X1), its piezo-electric effect generates several volts across the 10M resistor R3. This voltage triggers the CMOS timer IC1a, causing the piezo-electric horn (X2) to sound for a plastic housing that includes a driver circuit for producing a continuous tone at the transducer's resonant frequency, and IC1b modulates the signal by gating the horn on and off, which is comparable to the output of a typical smokedetector alarm.

The shock sensor is a piezo-electric "bender"--a thin brass disk with a smaller piezo element bonded in the center. Separate leads attach to the brass and to the piezo element. You mount the device according to whether your application requires sensitivity in the vertical axis only (Fig 6-19) or all three axes (Fig 6-20).

In the vertical-axis case, the bending weight is soldered to the sensor opposite its point of support to enhance sensitivity by amplifying the sensor's movement, generating higher voltage for a given shock, on the other hand, you should limit the sensor's range of motion, as shown, to avoid cracking the brittle piezo element. In either case, apply the soldering iron briefly to avoid damaging the brass-piezo bond.

To achieve 3-axis sensitivity, solder one edge of the disk to a stationary anchor such as the printed-circuit board, and solder a 1 1/4-in. bolt to the opposite edge (Fig 6-20). Add two nuts, jammed together to maintain position. Again, you can adjust the sensor's sensitivity by altering this weight position.

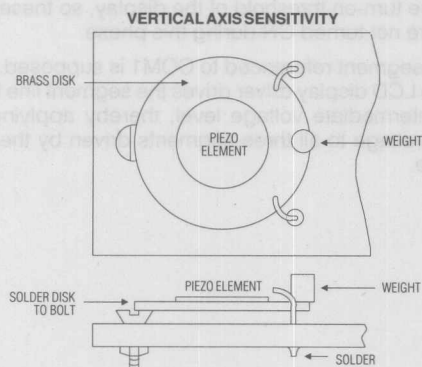


Figure 6-19. Built with two piezo-electric devices and one IC, this mechanical-shock produces a loud, pulsing alarm for one minute.

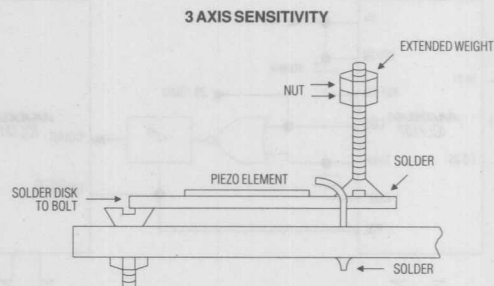


Figure 6-20. Mounting the piezo sensor in this manner (6-19) provides shock sensitivity primarily for motion normal to the pc board. Adding a cantilevered weight (6-20) provides sensitivity to applied motion in all three orthogonal axes.

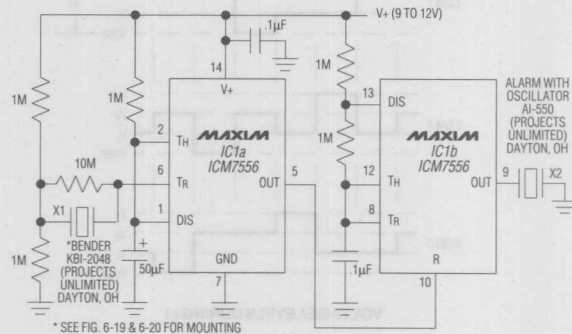


Figure 6-21.

Active Filters

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If a processor is not available, a MAX260/261/262 can be loaded from an EEPROM using some discrete logic. Toggle switches select the EEPROM address to be loaded and then the LOAD button transfers the data to the filter. With two filter ICs, any 8th-order filter function can be designed. The EEPROM must be preprogrammed with

the proper codes for the desired filter, but up to 256 separate filter designs can be stored in one memory chip. Pin numbers are shown for the MAX261/262. The MAX260 can also be used, but the pin numbers are somewhat different.

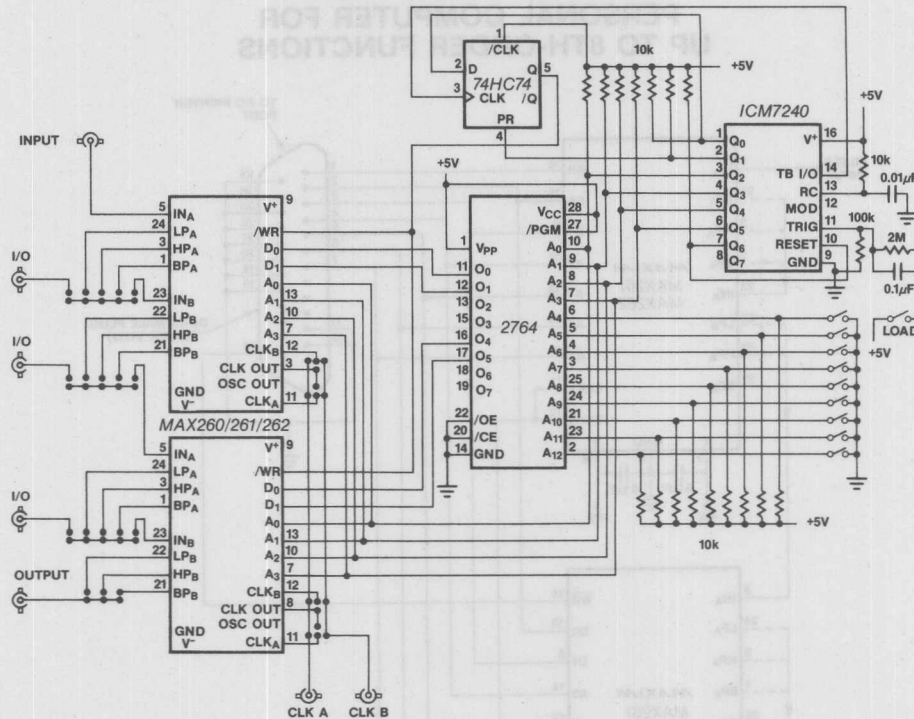


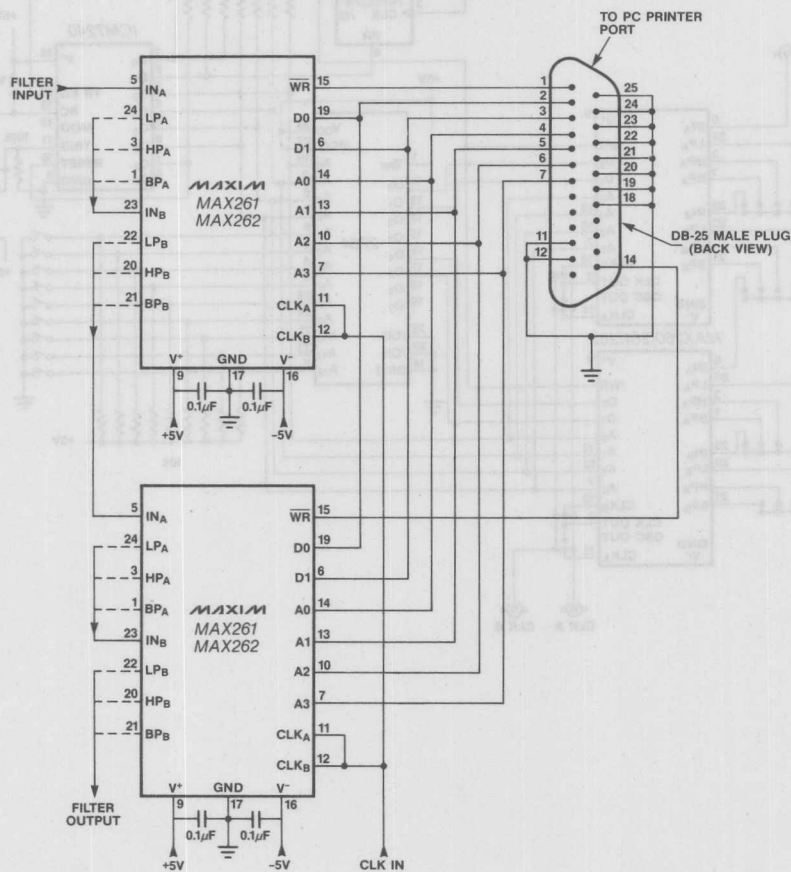
Figure 7-3.

Loading Filters From a Personal Computer for up to 8th-Order Functions

The MAX260, 261, and 262 are designed to be microprocessor programmed, however, for prototyping purposes, programming codes for f_{CLK}/f_c ratio, Q, and filter operating mode can be easily loaded into one or two filter ICs from a personal computer. The filter ICs are connected to the computer's parallel printer port as shown and the BASIC program listed loads programming data

directly to the chips. No interface circuitry is needed. The program asks for the filter programming codes and loads up to four 2nd-order sections in turn. Programming codes for specific filter designs can be generated by Maxim's filter design software or can be obtained from tables in the filter data sheets.

LOADING FILTERS FROM A PERSONAL COMPUTER FOR UP TO 8TH-ORDER FUNCTIONS



NOTE: PIN NUMBERS DIFFER FOR MAX 260. CONSULT DATA SHEET.

Figure 7-1.

This program asks for programming input instructions for up to 4 filter sections (up to 2 filter ICs). It asks for: MODE (Type in 1, 2, 3, or 4), CLOCK RATIO (f_{CLK}/f_0 , Type in 0 to 63), and Q (Type in 0 to 127). In the program prompts there are references to "TABLE 2", "TABLE 3", and "TABLE 5". These can be found in the MAX260/261/262 data sheet. Programming numbers can be taken from these tables or can be generated in Maxim's Filter Design Software.

The filter-loading BASIC program loops through all four filter sections in sequence. A section is loaded when the Q for that section is entered. Other sections remain unchanged when any one is reloaded. Also, the program does not "end" but merely waits for reprogramming data for the next section in the sequence. If no new instructions are entered, the filter's programmed state does not change.

```

10 PRINT "PRINTER PORT ADDRESS FOR LPT1:"
20 PRINT "          3BC   ( PORT ON DISPLAY ADAPTER )      =0 "
30 PRINT "          378   ( PORT NOT ON DISPLAY ADAPTER ) =1 ";
40 INPUT P : IF P>2 OR P<0 THEN 10
50 IF P=0 THEN PORT=956 ELSE PORT=888 ' SET PORT ADDRESS
60 FOR CHIP=1 TO 2
70 PRINT "CHIP # ";CHIP
80 AB$="FILTER A "
90 GOSUB 180 : REM GET DATA FOR SECTION A
100 ADD=0 : REM FILTER A ADDRESS
110 GOSUB 290 : REM WRITE DATA TO THE PRINTER PORT
120 AB$="FILTER B "
130 GOSUB 180 : REM GET DATA FOR SECTION B
140 ADD=32 : REM FILTER B ADDRESS
150 GOSUB 290 : REM WRITE DATA TO THE PRINTER PORT
160 NEXT
170 GOTO 60
180 PRINT "MODE (1 TO 4, SEE TABLE 5) "; AB$;
190 INPUT M
200 IF M<1 OR M>4 THEN 180
210 PRINT "CLOCK RATIO (0 TO 63, N OF TABLE 2) "; AB$;
220 INPUT F
230 IF F<0 OR F>63 THEN 210
240 PRINT "Q (0 TO 127, N OF TABLE 3) "; AB$;
250 INPUT Q
260 IF Q<0 OR Q>127 THEN 240
270 PRINT
280 RETURN
290 X=(ADD+M-1)
300 GOSUB 450
310 ADD=ADD+4
320 FOR I=1 TO 3
330 X=ADD+(F-4*INT(F/4))
340 GOSUB 450
350 F=INT(F/4)
360 ADD=ADD+4
370 NEXT I
380 FOR I=1 TO 4
390 X=ADD+(Q-4*INT(Q/4))
400 GOSUB 450
410 Q=INT(Q/4)
420 ADD=ADD+4
430 NEXT I
440 RETURN
450 '>>>>>> OUTPUT <<<<<<<<<<<<
460 OUT PORT,X
470 OUT PORT+2,CHIP
480 OUT PORT+2,0
490 RETURN

```

Figure 7-2.

MAX260 are cascaded. The f_0 and Q parameters for each section are:

$$f_{0A} = 3\text{kHz} \quad f_{0B} = 3\text{kHz}$$

$$Q_A = 1.307 \quad Q_B = 0.541$$

Mode 1 and a 400kHz clock are used. Because of low Q values, the sampling errors of one figure at end of section begin to look significant in this case. From the graphs in Figure 7-28 (Page 7-20), using f_{CLK}/f_0 ratio near 133, f_{0A} will be about 4% high, f_{0B} will be 1.5% high. Q_A will be -1.2% low, and Q_B will be -0.5% low. If these errors are not a problem, the corrections can be ignored. They are included here for best possible accuracy:

$$f_{CLK}/f_{0A} = 133.00 \text{ (N = 22), } f_{0B} = 2901 \text{ Hz}$$

$$(-1.3\% \text{ correction})$$

$$f_{CLK}/f_{0B} = 139.80 \text{ (N = 25), } f_{0A} = 2861 \text{ Hz}$$

$$(-4.6\% \text{ correction})$$

$$Q_A = 1.306 \text{ (N = 79, Q resolution prevents +0.5\% correction)}$$

$$Q_B = 0.547 \text{ (N = 11, +1.1\% correction)}$$

Measured wideband noise for this filter is $123\mu\text{V RMS}$. If Mode 2 were used, the noise would be $87\mu\text{V RMS}$. For lower noise with either Mode the first section should have the highest Q (Section A in this example).

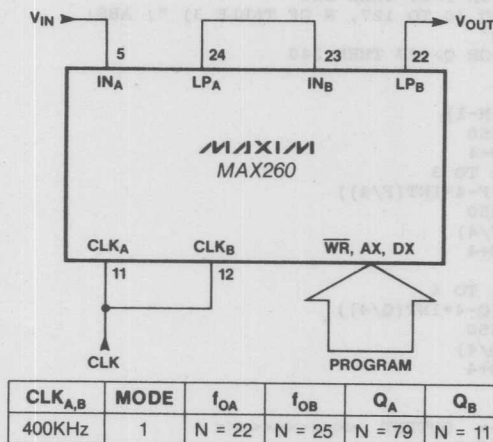
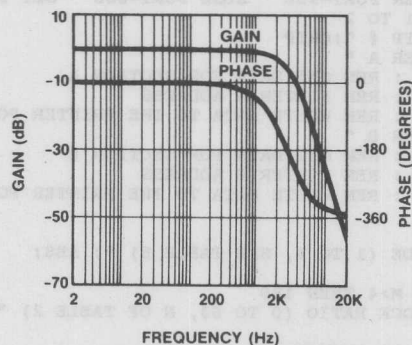


Figure 7-4.

Cutoff Frequency = 30kHz
 $f_{0A} = f_{0B} = 30\text{kHz}$
 $Q_A = 1.307$, $Q_B = 0.541$
 Gain = 1

The MAX266 works well in this application because of its high operating frequency. Since f_0 is the same for both 2nd-order sections, Mode 1 works well. The above "cook-book" f_0 and Q values for Butterworth filters can be used directly, or the filter design program, PZ, can be used.

If we arbitrarily pick a 2MHz clock for both sections, f_{CLK}/f_0 would be 66.7. By checking the sampling error graphs in Figure 7-28 (Page 7-20), however, we see errors approaching 9% at low f_{CLK}/f_0 ratio and low Q . The errors can either be corrected using the data from the graphs, or the filter software (Programs PZ and RP) can be used. The RP design program outputs (rounded to 3 digits here), with error corrections, are:

Sec#1: $R_1 = 20\text{k}\Omega$, $R_2 = 20\text{k}\Omega$, $R_3 = 26.6\text{k}\Omega$
 Programmed Clk Ratio = 69.12
 Clk Frequency = 2MHz

Sec#2: $R_1 = 35.9\text{k}\Omega$, $R_2 = 35.9\text{k}\Omega$, $R_3 = 20\text{k}\Omega$
 Programmed Clk Ratio = 72.26
 Clk Frequency = 2MHz

Note the different programmed clock ratios are selected by RP for each Mode 1 section because slightly different sampling error corrections are applied to each section. The MAX265/266 does not allow separate programming of each filter half (This is allowed by the MAX260/261/262. See appropriate data sheet.) so here we can:

- 1) Use a clock ratio of 69.12 in both halves and accept the resulting response error.
- 2) Use a ratio of 69.12 in both halves but change section #2's clock to $(69.12/72.26) \times 2\text{MHz} = 1.913\text{MHz}$ to correct for the error.
- 3) Use a ratio of 69.12 and a 2MHz clock in both halves but change section 2 to Mode 1B which allows f_0 to be raised with resistors.

We continue the design to demonstrate 3), so the above Mode 1 design for section 2 is changed to Mode 1B. This way the clock ratio of 72.26, which can't be set directly (since sections 1 and 2 are one value, 69.12) is tuned by R_5 and R_6 :

$$\frac{\text{Desired } f_{CLK}/f_0 \text{ of section 2}}{\text{Programmed } f_{CLK}/f_0 \text{ of sections 1 and 2}} = \sqrt{1 + R_6/(R_5 + R_6)}$$

$$72.26/69.12 = \sqrt{1 + R_6/(R_5 + R_6)} = 1.045$$

A side effect of tuning f_0 with resistors is that section 2's Q and gain also are shifted. They are restored to their original value (from the Mode 1 design above) by changing R_3 and R_1 as described below.

The Q of section 2 in Mode 1B is:

$$Q = (R_3/R_2) \sqrt{1 + R_6/(R_5 + R_6)} = 1.045 (R_3/R_2).$$

Dividing R_3 ($20\text{k}\Omega$) by 1.045 provides the value needed ($19.1\text{k}\Omega$) to compensate for the Q shift caused by R_5 and R_6 .

The gain of section 2 in Mode 1C is:

$$\text{HOLP} = -(R_2/R_1)/(1 + R_6/(R_5 + R_6)) = -1.092 (R_2/R_1)$$

Multiplying R_1 ($35.9\text{k}\Omega$) by 1.092 provides the value needed ($39.2\text{k}\Omega$) to compensate for the gain shift caused by R_5 and R_6 . Figure 7-5 shows the connection and response for the complete filter. The final design values are tabulated below, but the resistors may be scaled to other values as long as the ratios are maintained.

Sec#1: $R_1 = 20\text{k}\Omega$, $R_2 = 20\text{k}\Omega$, $R_3 = 26.6\text{k}\Omega$
 Programmed Clk Ratio = 69.12
 Clk Frequency = 2MHz

Sec#2: $R_1 = 39.2\text{k}\Omega$, $R_2 = 35.9\text{k}\Omega$, $R_3 = 19.1\text{k}\Omega$
 $R_5 = 20\text{k}\Omega$, $R_6 = 2.04\text{k}\Omega$
 Programmed Clk Ratio = 69.26
 Clk Frequency = 2MHz

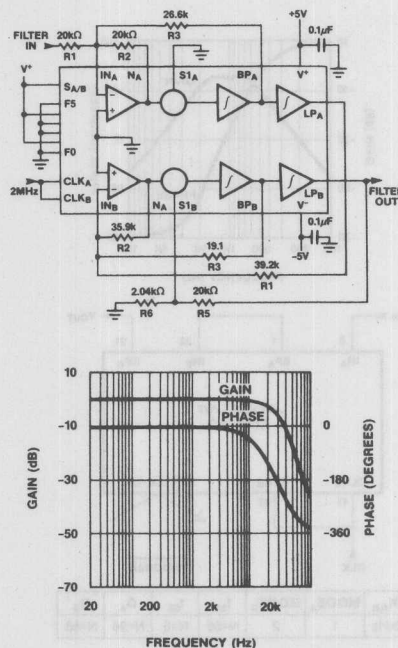


Figure 7-5. 30kHz Butterworth Lowpass with 2MHz Clock

In this example the desired parameters are:

Center frequency (f_0)	= 1 kHz
Pass bandwidth	= 1 kHz
Stop bandwidth	= 3 kHz
Max passband ripple	= 1 dB
Min stopband Attenuation	= 20 dB

From the above parameters, we use either lookup tables, design texts or Maxim's filter design programs to generate the order (number of poles), and the f_0 and Q of each second-order section. The A and B parameters are:

f_{0A} = 639 Hz	f_{0B} = 1564 Hz
Q_A = 2.01	Q_B = 2.01

To implement this filter, section A operates in Mode 1 and section B uses Mode 2 to provide a wider overall range of f_{CLK}/f_0 ratios. This way one clock frequency can drive both sections A and B. See selection Tables 2 and 3 of MAX260 data sheet.

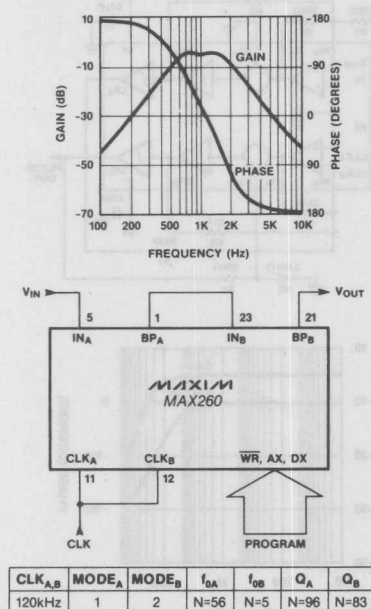


Figure 7-6. Wide Passband Chebyshev Bandpass Filter

CLK _A = CLK _B = 120 kHz
f_{CLK}/f_{0A} = 188.49 (Mode 1, N = 56), actual f_{0A} = 636.6 Hz
f_{CLK}/f_{0B} = 76.64 (Mode 2, N = 5), actual f_{0B} = 156.5 Hz
Q_A = 2.000 (Mode 1, N = 96), Q_B = 2.01 (Mode 2, N = 83)

The overall passband gain at f_0 will be 0.64V/V or -3.9dB.

The same Chebyshev response shape shown in Figure 7.6 is implemented at higher frequencies with a MAX262 in Figure 7-7. The curves show plots for center frequencies of 15.6kHz, 31.3kHz, and 47kHz. Not only is this faster than the MAX260 implementation but Mode 1 can be used on both halves of the MAX262 for this filter because the range of available f_{CLK}/f_0 ratios is wider with the MAX262 than the MAX260.

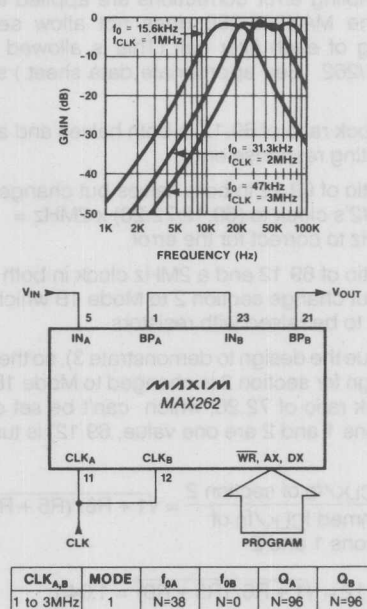


Figure 7-7. High Frequency Chebyshev Bandpass Filter

4th-Order Chebyshev Bandpass Filter (MAX260)

Here both halves of a MAX260 are cascaded to form a fourth-order Chebyshev bandpass filter. The desired parameters are:

Center frequency (f_0)	= 1kHz
Pass bandwidth	= 200 Hz
Stop Bandwidth	= 600 Hz
Max. passband ripple	= 0.5 dB
Min. stopband Attenuation	= 15 dB

From the above parameters, the order (number of poles), and the f_0 and Q of each section can be determined. Such a derivation is beyond the scope of this note, however there are a number of sources which provide design data for this procedure. These include look-up tables, design texts and computer programs. Design software is available from Maxim to provide comprehensive solution for most popular filter configurations. The A and B section parameters for the above filter are:

$f_{0A} = 904$ Hz	$f_{0B} = 1106$ Hz
$Q_A = 7.05$	$Q_B = 7.05$

To implement this filter, both halves operate in Mode 1 and use the same clock. See selection Tables 2 and 3. The programmed parameters are:

$$CLK_A = CLK_B = 150 \text{ kHz}$$

$$f_{CLK}/f_{0A} = 166.50 \text{ (Mode 1, } N = 42\text{), actual } f_{0A} = 902.4 \text{ Hz}$$

$$f_{CLK}/f_{0A} = 136.66 \text{ (Mode 1, } N = 23\text{), actual } f_{0B} = 1099.7 \text{ Hz}$$

$$Q_A = Q_B = 7.11 \text{ (Mode 1, } N = 119\text{)}$$

Sampling errors are very small at this f_{CLK}/f_0 ratio so the actual realized Q is very close to 7.05 (See Figure 7-27 or Filter Program MPP). Often the realized Q will not be exactly the target value at high Q s because programing resolution lowers as Q increases. This doesn't affect most filter designs, since 3-digit Q accuracy is practically never required, and a Q resolution of 1 is provided up to Q s of 10. The overall filter gain at f_0 is 16.4V/V or 24.3dB (See Cascading Filters section). If another gain is required, amplification or attenuation must be added at the input, output, or between stages.

In Figure 7-9, a series of response curves are shown for the above configuration using a MAX261 with clock frequencies ranging from 750kHz to 4MHz f_0 from 500Hz to 30kHz). Note that the rightmost curve shows about 2dB of gain peaking compared to the lower frequency curves, indicating the upper limit of usable filter accuracy at this Q .

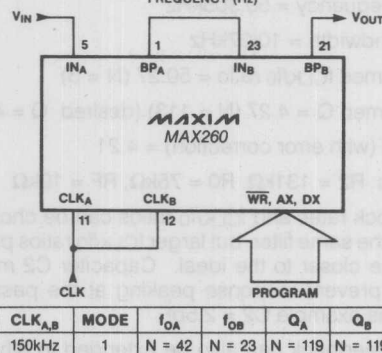
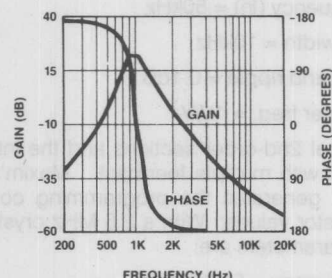


Figure 7-8. 4th-Order Chebyshev Bandpass Filter

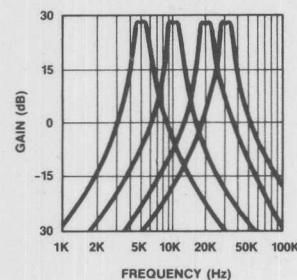


Figure 7-9. MAX261 4th-Order Chebyshev Bandpass Filter Using Coefficients of Figure 7-8.

Here a pin-programmed MAX268 operates as a 4th-order 50kHz Chebyshev bandpass filter. The specifications are:

Center frequency (f_0) = 50kHz

Pass bandwidth = 10kHz

Max. passband ripple = 0.1dB

Gain at center freq. = 1V/V

Two identical 2nd-order sections and the internal op amp are used with multiple feedback. Maxim's design program, BP, generates the programming codes and feedback resistor values. With a 2.5 MHz crystal clock, the realized parameters are:

Center frequency = 50.305kHz

Pass Bandwidth = 10.07kHz

Programmed f_{CLK}/f_0 ratio = 50.27 ($N = 3$)

Programmed $Q = 4.27$ ($N = 113$) (desired $Q = 4.215$)

Actual Q (with error correction) = 4.21

Resistors: $R_2 = 131k\Omega$, $R_0 = 75k\Omega$, $R_F = 10k\Omega$

Other clock rates and f_{CLK}/f_0 ratios can be chosen to implement the same filter, but larger f_{CLK}/f_0 ratios provide performance closer to the ideal. Capacitor C_2 may be needed to prevent response peaking at the passband edge. In this example $C_2 = 2.5pF$.

Multiple feedback can also be extended to 8th-order designs while still using one clock by adding a second MAX268 and 2 additional feedback resistors. These can also be calculated with the design program, BP. Note that for filter order above 4, the feedback signal from odd filter sections is inverted before it is summed.

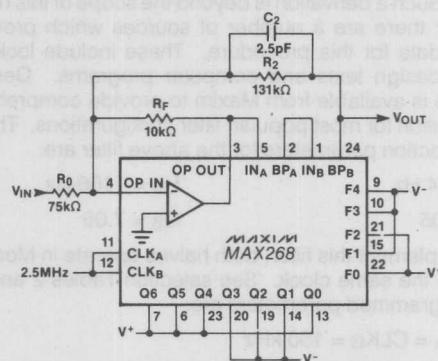
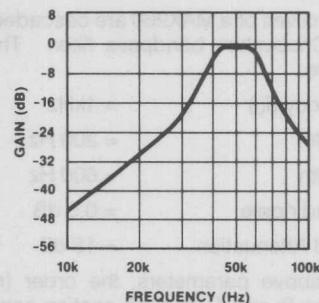


Figure 7-10. 4th-Order 50kHz Chebyshev Bandpass Using Multiple Feedback

Without multiple feedback, the previous example can be implemented with no external components; however, separate clocks are required for CLKA and CLKB. The target specifications are the same as before. The realized parameters are now:

CLKA = 1.89MHz, CLKB = 2.5MHz

Center frequency = 50kHz

Pass bandwidth = 10kHz

Programmed f_{CLK}/f_0 ratio = 43.98 ($N = 1$)

Programmed $Q = 4.27$ ($N = 113$) (desired $Q = 4.215$)

Actual Q (with error correction) = 4.2

With the chosen f_{CLK}/f_0 ratio, a crystal may be used at CLKA while a divided system clock, if available (2.5, 5, 10, or 20MHz), drives CLKB. This is suggested because CLKA has internal circuitry to drive a crystal while CLKB does not. Other clock sources may be used with a different programmed f_{CLK}/f_0 as long as the ratio between CLKA and CLKB remains the same as above. Another advantage of this circuit is that higher center frequencies can be achieved relative to equivalent multiple feedback designs because lower Q sections are used compared to multiple feedback.

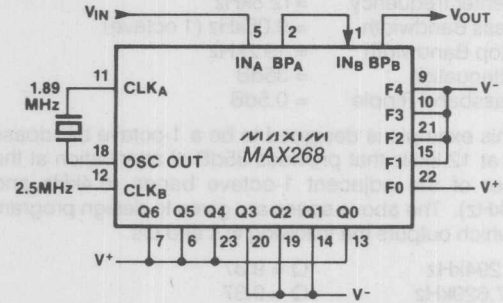
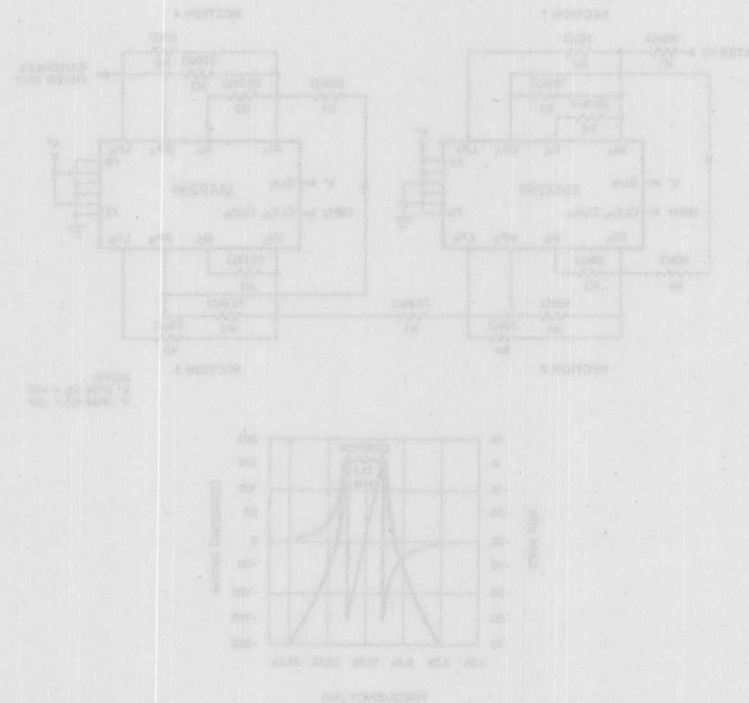


Figure 7-11. 4th-Order 50kHz Chebyshev Bandpass Using No External Resistors



Center frequency	= 12.8kHz
Pass Bandwidth	= 9.05kHz (1 octave)
Stop Bandwidth	= 19.2kHz
Attenuation	= 35dB
Passband Ripple	= 0.5dB

This example is designed to be a 1-octave bandpass filter at 12.8kHz that provides 35dB of attenuation at the center of the adjacent 1-octave bands (6.4kHz and 25.6kHz). The above specs are given to design program PZ which outputs the following f_0 's and Q s.

9.294kHz	$Q = 9.37$
17.629kHz	$Q = 9.37$
11.178kHz	$Q = 3.73$
14.657kHz	$Q = 3.73$

Two MAX266 ICs make the 8th-order filter. A 1MHz clock is preferred for all sections so filter Mode 3, which allows the most flexible tuning of f_0 and Q , is selected. Program RP picks resistors and programmed clock ratios. It asks for each section's f_0 , Q , f_{CLK} , and gain. All sections are set for a gain of one.

Program RP asks for: 1) clock frequency, 2) clock ratio, or 3) both as input data for each filter half, but in the MAX265,266 both halves use the same clock ratio. Therefore when designing section 1, we tell RP the clock frequency (1MHz) and ask the program to pick the clock ratio

to be the same as section 1. In section 3 (the second filter chip), the program picks the ratio, and we use this same ratio for section 4. As the circuit connection shows, the order of the sections is changed so that those with the closest f_0 are in the same IC. This way f_0 is tuned the least amount by resistors. The design values are listed below. Remember that these may be scaled to other values if the ratios are maintained.

Sec#1: $R_1 = 189k\Omega$, $R_2 = 20.2k\Omega$, $R_3 = 189k\Omega$
 $R_4 = 20k\Omega$
 Programmed Clk Ratio = 108.38
 Clk Frequency = 1MHz

Sec#2: $R_1 = 90k\Omega$, $R_2 = 29k\Omega$, $R_3 = 90k\Omega$
 $R_4 = 20k\Omega$
 Programmed Clk Ratio = 108.38
 Clk Frequency = 1MHz

Sec#3: $R_1 = 75.6k\Omega$, $R_2 = 20.2k\Omega$, $R_3 = 75.6k\Omega$
 $R_4 = 20k\Omega$
 Programmed Clk Ratio = 69.12
 Clk Frequency = 1MHz

Sec#4: $R_1 = 229k\Omega$, $R_2 = 29.5\Omega$, $R_3 = 229k\Omega$
 $R_4 = 20k\Omega$
 Programmed Clk Ratio = 108.38
 Clk Frequency = 1MHz

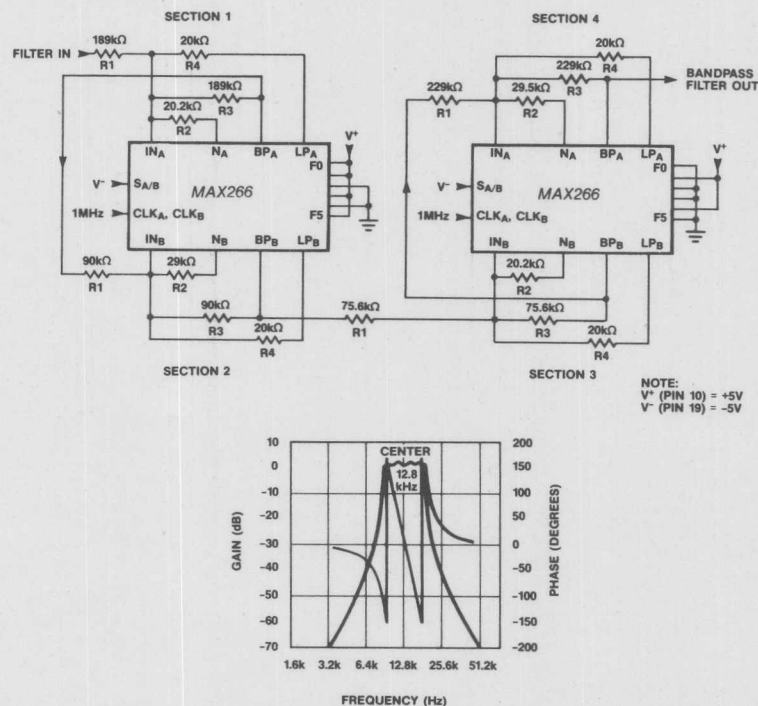


Figure 7-12. 12.8kHz, 1-Octave Bandpass with 1MHz Clock

Two Butterworth lowpass filters are set up to accurately track each other. By "splitting" two MAX263s, only one clock is needed. The specifications are:

Cutoff frequency = 3kHz

$f_{0A} = f_{0B} = 3\text{kHz}$

$Q_A = 1.307$, $Q_B = 0.541$

These values can be programmed directly into the filter. However, since the Q s are low, sampling errors may be large enough to deserve attention. From Figure 7-28 (Page 7-20), if f_{CLK}/f_0 is near 130 (f_{CLK} is 400kHz), f_{0A} and f_{0B} will be about 4% and 1.5% high respectively. Q_A and Q_B will be 1.2% and 0.5% low. These errors may not be large enough to worry about but are corrected here

(within the programming resolution of the MAX263) by the filter design programs PZ and MPP. f_{0A} and f_{0B} are programmed to different values ($N_A = 11$, $N_B = 12$) for this reason.

Mode 1, $CLK_A = CLK_B = 400\text{kHz}$

$f_{CLK}/f_{0A} = 135.08$, $N = 11$

(target $f_{0A} = 2961\text{Hz}$, actual = 3008Hz)

$f_{CLK}/f_{0B} = 138.23$, $N = 12$

(target $f_{0B} = 2894\text{Hz}$, actual = 3015Hz)

$Q_A = 1.31$, $N = 79$ (actual $Q_A = 1.30$)

$Q_B = 0.547$, $N = 11$ (actual $Q_B = 0.542$)

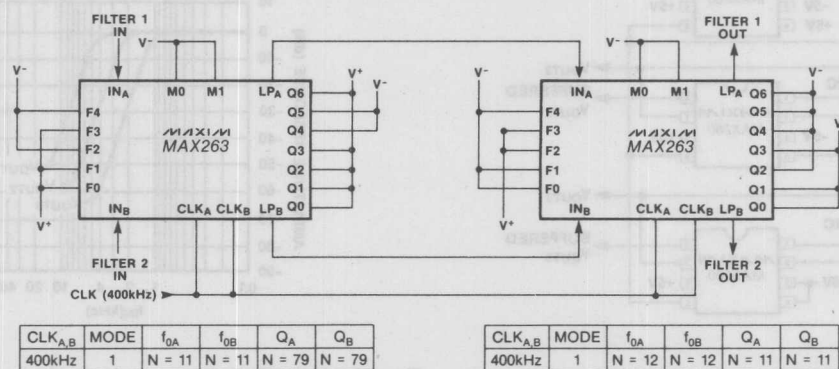
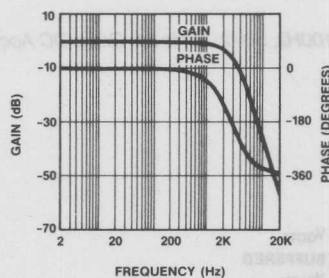


Figure 7-13. Dual Tracking 3kHz 4th-Order Lowpass

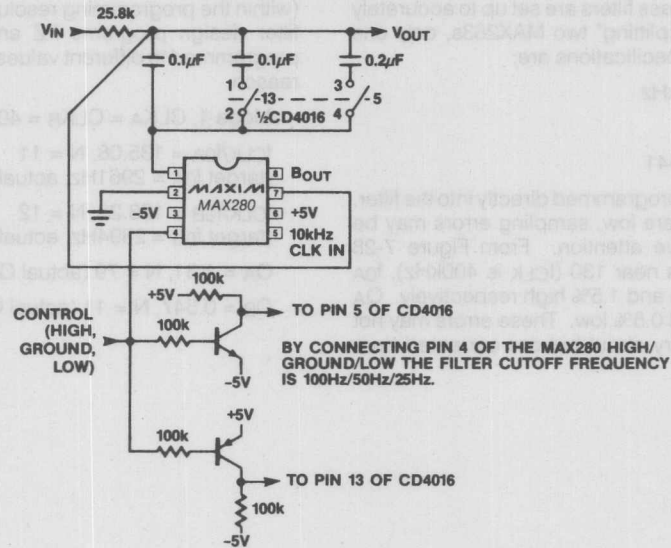


Figure 7-14. 100Hz, 50Hz, 25Hz 5th Order DC Accurate LP Filter

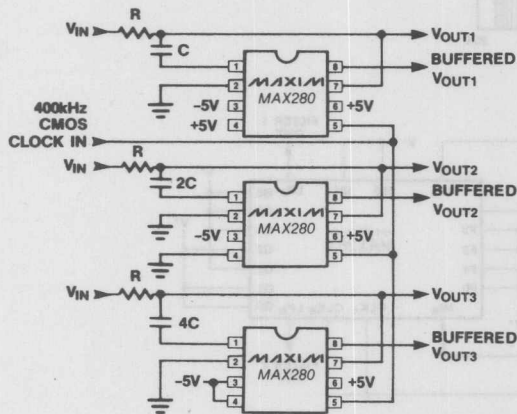


Figure 7-15. Octave Tuning with a Single Input Clock

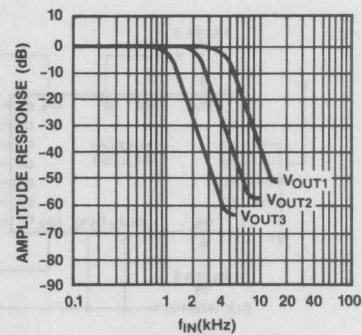


Figure 7-16. Amplitude Response for the Octave Tuning Circuit

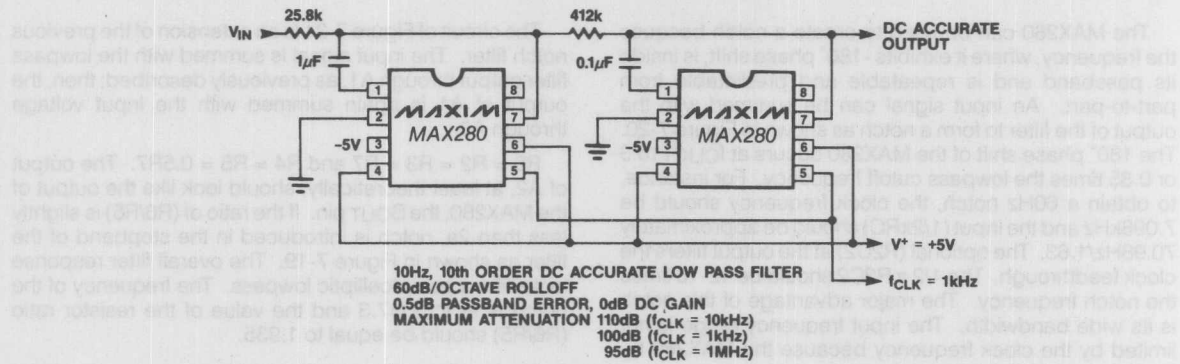


Figure 7-17. Simple Cascading Technique

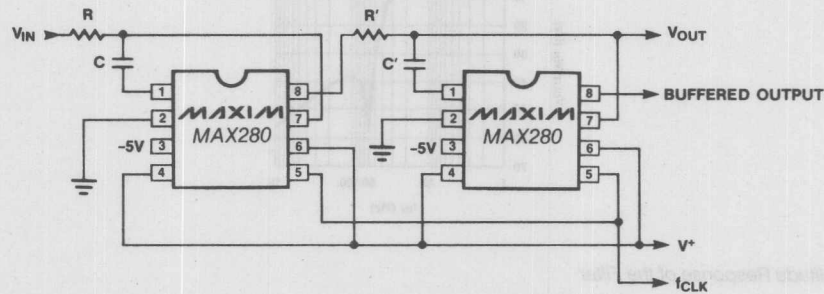


Figure 7-18. Cascading Two MAX280s. The 2nd Stage is Driven by the Buffered Output of the First Stage.

The MAX280 can be used to create a notch because the frequency, where it exhibits -180° phase shift, is inside its passband and is repeatable and predictable from part-to-part. An input signal can be summed with the output of the filter to form a notch as shown in Figure 7-20. The 180° phase shift of the MAX280 occurs at $f_{CLK}/118.3$ or 0.85 times the lowpass cutoff frequency. For instance, to obtain a 60Hz notch, the clock frequency should be 7.098kHz and the input $(1/2\pi RC)$ should be approximately $70.98\text{Hz}/1.63$. The optional $(R2C2)$ at the output filters the clock feedthrough. The $1/2\pi R2C2$ should be 12-15 times the notch frequency. The major advantage of this notch is its wide bandwidth. The input frequency range is not limited by the clock frequency because the MAX280 by itself does not alias.

The circuit of Figure 7-21 is an extension of the previous notch filter. The input signal is summed with the lowpass filter output through A1, as previously described; then, the output of A1 is again summed with the input voltage through A2.

$R6 = R2 = R3 = R7$ and $R4 = R5 = 0.5R7$. The output of A2, at least theoretically, should look like the output of the MAX280, the BOUT pin. If the ratio of $(R6/R5)$ is slightly less than 2a, notch is introduced in the stopband of the filter as shown in Figure 7-19. The overall filter response looks like a pseudoelliptic lowpass. The frequency of the notch is at $f_{CLK}/47.3$ and the value of the resistor ratio $(R6/R5)$ should be equal to 1.935.

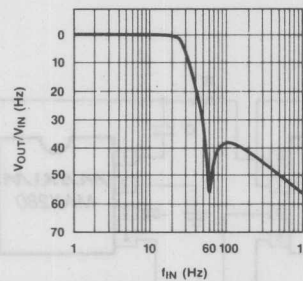


Figure 7-19. Amplitude Response of the Filter

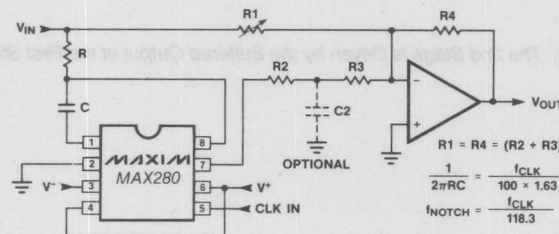


Figure 7-20. Using the MAX280/LTC1062 to Create a Notch

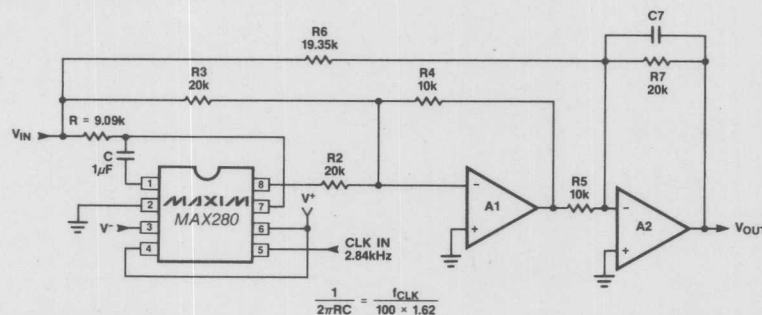
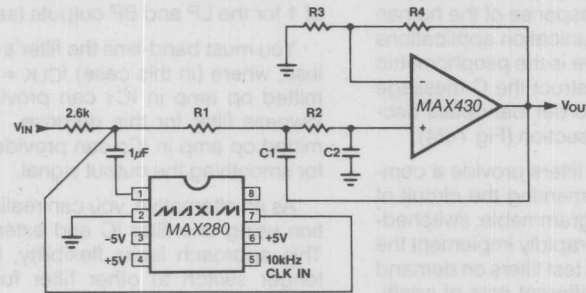


Figure 7-21. A low pass Filter with a 60Hz Notch



THE MAX430 IS CONNECTED AS A 2nd ORDER SALLEN KEY LOWPASS FILTER WITH A CUTOFF FREQUENCY EQUAL TO THE MAX280. THE ADDITIONAL FILTERING ELIMINATES ANY 10kHz CLOCK FEED THROUGH PLUS DECREASES THE WIDEBAND NOISE OF THE FILTER.

DC OUTPUT OFFSET (REFERRED TO A DC GAIN OF UNITY) = 5μV Max.

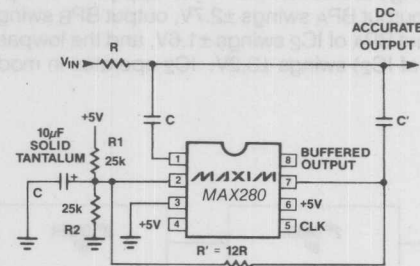
WIDEBAND NOISE (REFERRED TO A DC GAIN OF UNITY) = 60μV/RMS

OUTPUT FILTER COMPONENT VALUES						
DC GAIN	R3	R4	R1	R2	C1	C2
1	∞	0	14.3k	53.6k	0.1μF	0.033μF
10	3.57k	32.4k	4.6k	27.4k	0.1μF	0.2μF
101	0.324	32.4k	0.31k	16.9k	0.47μF	1μF

Figure 7-22. 7th-Order 100Hz Lowpass Filter with Continuous Output Filtering, Output Buffering and Gain Adjustment

MAX280/MAX281 Single Supply Operation

The MAX280/MAX281 can be operated with a single power supply. The AGND pin and the OUT pin should be biased at 1/2 supply. The value of the resistors R1 and R2 should be chosen to conduct 100μA or more. R' DC biases the buffer and C' isolates the buffer from the DC value of the output. Under these conditions the external resistor and capacitor should be adjusted such that $(1/2 \pi RC) = f_c/1.84$. This accounts for the extra loading of the R', C' combination. R' and C' are not required if the input voltage has a DC value around 1/2 supply. If an external capacitor is used to activate the internal oscillator, its bottom plate should be tied to system ground. The AGND pin should also be bypassed by a decoupling capacitor.



FOR A 10Hz FILTER $R = 29.4k\Omega$, $C = 1\mu F$, $f_{CLK} = 1kHz$

THE FILTER IS MAXIMALLY FLAT FOR $\frac{1}{2\pi RC} = \frac{f_c}{1.84}$

Figure 7-23. Single 5V Supply 5th Order LP Filter

The C-message filter is a commonly specified test and measurement filter that simulates response of the human ear for voice, audio, and telecommunication applications in the U.S. In Europe, a close relative is the psophometric noise-weighting filter. You can construct the C-message filter, by cascading three second-order bandpass sections with a second-order lowpass section (Fig 7-24).

Dual universal, second-order IC filters provide a compact and efficient means for implementing the circuit of Fig 7-24. If the IC filters are also programmable, switched-capacitor types as shown, you can rapidly implement the C-message, psophometric, or other test filters on demand simply by loading the chips with different sets of coefficients. These coefficients set each 2nd-order section's filter mode, Q, and cutoff or center frequency f_0 . The C-message filter has poles only, which are specified by the IEEE Standard 743-1984:

Pole	Value in rad/sec	Value in Hz (f_0)	Q
BP#1	$-1502 \pm j1267$	312.741	0.6540
BP#2	$-2439 \pm j5336$	933.761	1.2027
BP#3	$-4690 \pm j15267$	2541.886	1.7026
LP#1	$-4017 \pm j21575$	3492.778	2.7316

Fig 7-25 shows the external connections that configure two MAX262s in the filter architecture of Fig 7-24. Fig 7-25 also lists decimal equivalents of the digital coefficients required to program for each filter section. For the maximum signal-to-noise ratio, signal amplitudes at the 2nd-order section outputs should be as high as possible.

Signal swings are as follows: If you apply $\pm 4V$ to input INA on IC1, output BPA swings $\pm 2.7V$, output BPB swings $\pm 1.85V$, output BPA of IC2 swings $\pm 1.6V$, and the lowpass output (LPA of IC2) swings $\pm 3.2V$. IC2 operates in mode

4 instead of mode 1, which provides a gain of 2 instead of 1 for the LP and BP outputs (see data sheet).

You must band-limit the filter's input signal to $f_{CLK}/4$ or less, where (in this case) $f_{CLK} = 38.4$ kHz. The uncommitted op amp in IC1 can provide a 2nd- or 3rd-order lowpass filter for this purpose. If needed, the uncommitted op amp in IC2 can provide a similar lowpass filter for smoothing the output signal.

As an alternative, you can realize the C-message function using one filter IC and external op amp (Fig 7-26). This approach lacks flexibility, however. You can no longer switch to other filter functions by electrically reprogramming the circuit.

This circuit realizes the first bandpass (BP#1) in terms of external resistors and capacitors around the uncommitted op amp of IC1. BP#1, which also serves as an antialiasing filter for the sampling action of IC1, is an infinite-gain, multiple-feedback bandpass filter with $f_0 = 312.74$ Hz, $Q = 0.654$, and gain = 0.654. Design procedures for this configuration are available in the literature. (Johnson & Holburn, "Rapid practical designs of active filters", John Wiley & Sons.)

IC2 implements BP#2 and BP#3 with the same gain and signal levels as in Fig 7-24. The external op amp with resistors and capacitors implements LP#1, which also serves as the output smoothing filter. Like BP#1, you can design LP#1 as an infinite-gain, multiple-feedback circuit with $f_0 = 3492.778$, $Q = 2.7316$, and gain = 2.

The 125-kHz clock frequency is arbitrary; other values require that you program IC1 for a different f_{CLK}/f_0 ratio. In both filter circuits (Fig 7-24 and Fig 7-25) the coefficients for f_0A , f_0B , QA , and QB were calculated by software available from Maxim (see data sheet). Fig 7-28 shows the filter transfer function for either realization.

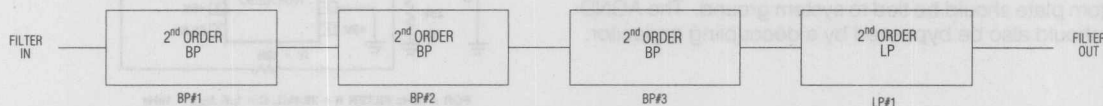
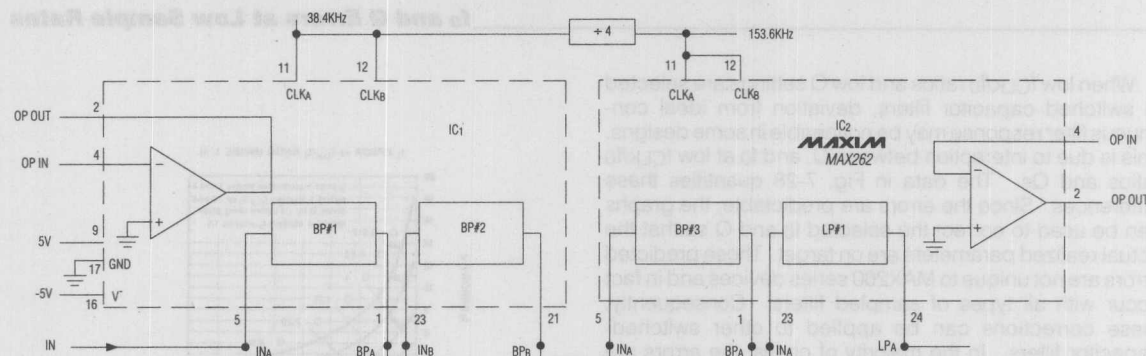


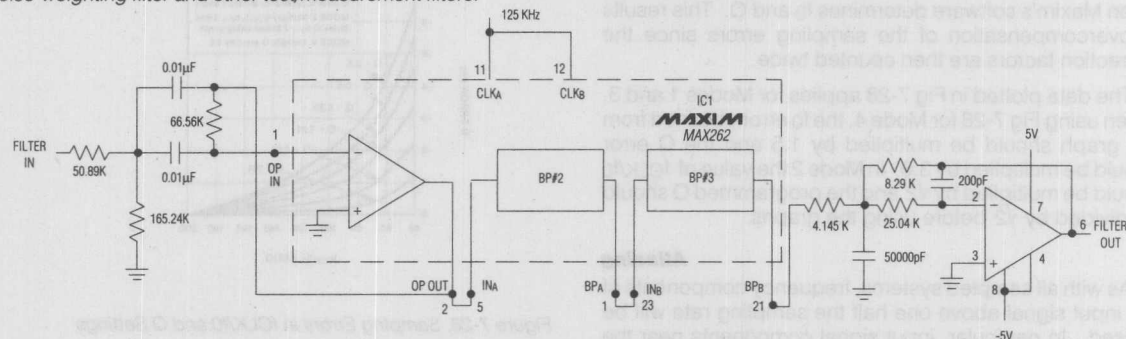
Figure 7-24. Cascaded, 2nd-order universal filter sections implement a C-message filter.



ModeA	ModeB	f _{0A}	f _{0B}	Q _A	Q _B
1	1	N = 55	N = 2	N = 31	N = 76

ModeA	ModeB	f _{0A}	f _{0B}	Q _A	Q _B
4	4	N = 13	N = 3	N = 91	N = 105

Figure 7-25. The circuit connections and coefficient sets shown enable two programmable, switched-capacitor filter ICs to realize the C-message filter of Fig 7-24. By loading the ICs with different coefficient sets, you can obtain the European psophometric noise-weighting filter and other test/measurement filters.



CLKA	CLKB	ModeA	ModeB	f _{0A}	f _{0B}	Q _A	Q _B
125kHz	125kHz	1	4	N = 61	N = 6	N = 75	N = 91

Figure 7-26. This circuit, based on one filter IC and an external op amp, produces the same C-message response of Figure 7-24, but lacks programming flexibility.

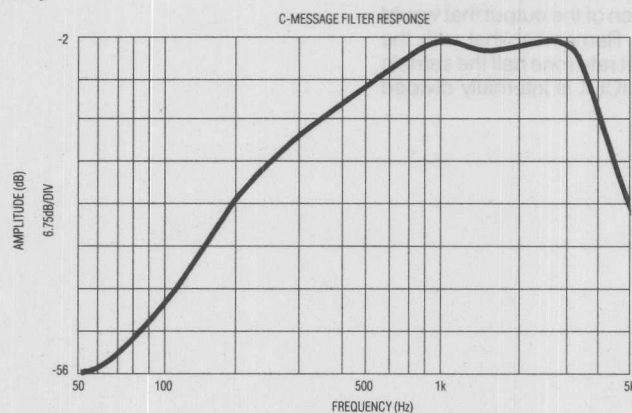


Figure 7-27. Circuits of Figure 7-24 and Figure 7-25 produce the same frequency response.

When low f_{CLK}/f_0 ratios and low Q settings are selected in switched capacitor filters, deviation from ideal continuous filter response may be noticeable in some designs. This is due to interaction between Q, and f_0 at low f_{CLK}/f_0 ratios and Qs. The data in Fig. 7-28 quantifies these differences. Since the errors are predictable, the graphs can be used to correct the selected f_0 and Q so that the actual realized parameters are on target. These predicted errors are not unique to MAX260 series devices and in fact occur with all types of sampled filters. Consequently, these corrections can be applied to other switched-capacitor filters. In the majority of cases, the errors are not significant, i.e. less than 1%, and correction is not needed. However, the MAX262 does employ a lower range of f_{CLK}/f_0 ratios than the MAX260 or MAX261 and is more prone to sampling errors as the tables show.

Maxim's filter design software applies the previous corrections automatically as the function of desired f_{CLK}/f_0 , and Q. Therefore, Fig 7-28 should NOT be used when Maxim's software determines f_0 and Q. This results in overcompensation of the sampling errors since the correction factors are then counted twice.

The data plotted in Fig 7-28 applies for Modes 1 and 3. When using Fig 7-28 for Mode 4, the f_0 error obtained from the graph should be multiplied by 1.5 and the Q error should be multiplied by 3.0. In Mode 2 the value of f_{CLK}/f_0 should be multiplied by $\sqrt{2}$ and the programmed Q should be divided by $\sqrt{2}$ before using the graphs.

Aliasing

As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. In particular, input signal components near the sampling rate generate difference frequencies that often fall within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, ($f_{CLK} = 200\text{kHz}$) is 1kHz. This waveform is an attenuated version of the output that would result from a true 1kHz input. Remember that with the MAX260 series filters, the nyquist rate (one half the sample rate) is in fact $f_{CLK}/4$ because f_{CLK} is internally divided by two.

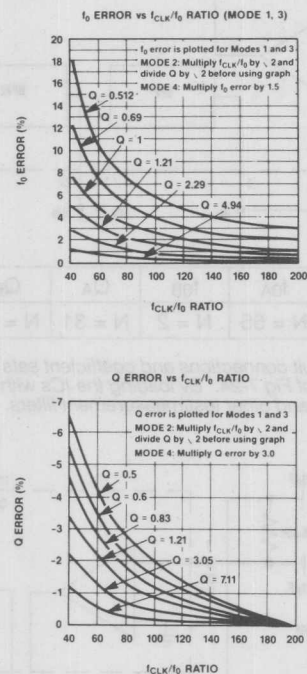


Figure 7-28. Sampling Errors in f_{CLK}/f_0 and Q Settings

A Primer on Switched-Capacitor Filters

Ease of use has made integrated, switched-capacitor filters attractive for many new applications. This article can help you prepare for such designs by describing the filter products and by explaining the concepts that govern their operation.

Starting with a simple integrator, we first develop an intuitive approach to active filters in general and then introduce practical realizations such as the state-variable filter and its implementation in switched-capacitor form. Specific integrated filters mentioned include the MF10 and Maxim's new microprocessor-programmable MAX260 family.

First Order Filters

An integrator (Figure 1a) is the simplest filter mathematically, and it forms the building block for most modern integrated filters. Consider what we know intuitively about an integrator. If you apply a DC signal at the input (i.e., zero frequency), the output will describe a linear ramp that grows in amplitude until limited by the power supplies. Ignoring that limitation, the response of an integrator at zero frequency is infinite, which means that it has a pole at zero frequency. (A pole exists at any frequency for which the transfer function's value becomes infinite.)

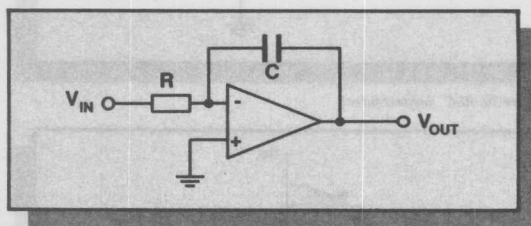


Figure 1a. Simple RC Integrator

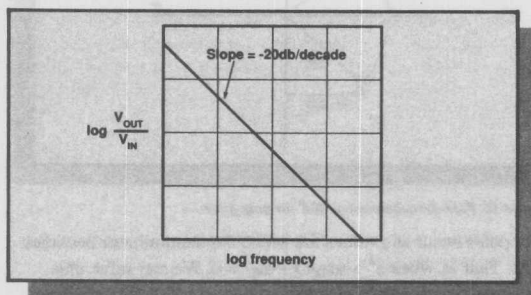


Figure 1b. Bode plot of simple integrator

We also know that the integrator's gain diminishes with increasing frequency, and that at high frequencies the output voltage becomes virtually zero. Gain is inversely proportional to frequency, so it has a slope of -1 when plotted on log/log coordinates (i.e., -20db/decade on a Bode plot, Figure 1b).

You can easily derive the transfer function as

$$\frac{V_{OUT}}{V_{IN}} = \frac{X_C}{R} = \frac{1/sC}{R} = \frac{\omega_0}{s}$$

where s is the complex-frequency variable $\sigma + j\omega$, and ω_0 is $1/RC$. If we think of s as frequency, this formula confirms the intuitive feeling that gain is inversely proportional to frequency. We will return to integrators later, in discussing the implementation of actual filters.

The next most complex filter is the simple lowpass RC type. (Figure 2a) Its characteristic (transfer function) is

$$\frac{V_{OUT}}{V_{IN}} = \frac{1/sC}{R + 1/sC} = \frac{1}{1 + sCR} = \frac{\omega_0}{s + \omega_0}$$

When $s = 0$ the function reduces to ω_0/ω_0 , i.e. 1. When s tends to infinity the function tends to zero, so this is a lowpass filter.

When $s = -\omega_0$ the denominator is zero and the function's value is infinite, indicating a pole in the complex frequency plane.

The magnitude of the transfer function is plotted against s in Figure 2b, where the real component of s (σ) is towards us, and the positive imaginary part ($j\omega$) is toward the right. The pole at $-\omega_0$ is evident. Amplitude is shown logarithmically to emphasize the function's form. For both the integrator and the R-C lowpass filter, frequency response tends to zero at infinite frequency. That is, there is a zero at $s = \infty$. This single zero surrounds the complex plane.

But how does the complex function in s relate to the circuit's response to actual frequencies? When analyzing the response of a circuit to AC signals, we use the expression $j\omega L$ for impedance of an inductor and $1/j\omega C$ for that of a capacitor. When analyzing transient response using Laplace transforms, we use sL and $1/sC$ for the impedances of these elements. The similarity is immediately apparent. The $j\omega$ in AC analysis is in fact the imaginary part of s , which, as mentioned earlier, is composed of a real part s and an imaginary part $j\omega$.

If we replace s by $j\omega$ in any equation so far, we have the circuit's response to an angular frequency ω . In the complex plot of Figure 2b, $\sigma = 0$ and hence $s = j\omega$ along the positive $j\omega$ axis, so the function's value along this axis is the frequency response of the filter. We have sliced the function along the $j\omega$ axis, and emphasized the RC lowpass filter's frequency-response curve by adding a heavy line for function values along the positive $j\omega$ axis. The more familiar Bode plot (Figure 2c) looks different in form only because the frequency is expressed logarithmically.

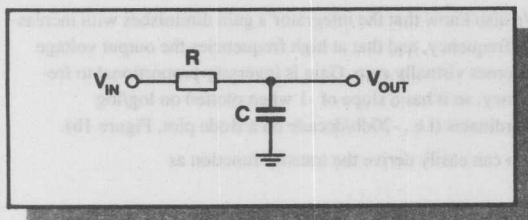


Figure 2a. Simple RC lowpass filter

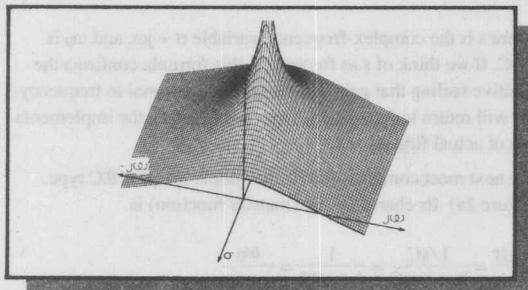


Figure 2b. Complex function of RC lowpass filter

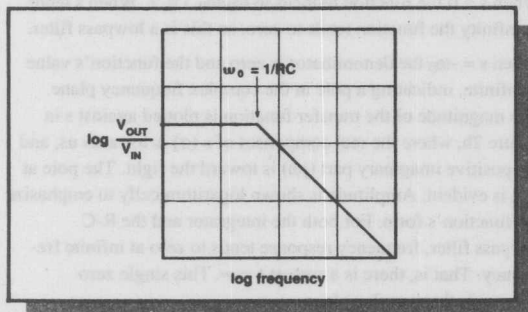


Figure 2c. Bode plot of lowpass filter

While the complex frequency's imaginary part ($j\omega$) helps describe a response to AC signals, the real part (σ) helps describe a circuit's transient response. Looking at Figure 2b, we can therefore say something about the RC lowpass filter's response as compared to that of the integrator. The lowpass filter's transient response is more stable because its pole is in the negative-real half of the complex plane.

That is, the lowpass filter makes a decaying-exponential response to a step-function input; the integrator makes an infinite response. For the lowpass filter, pole positions further down the $-\sigma$ axis mean a higher ω_0 , a shorter time constant, and therefore a quicker transient response. Conversely, a pole closer to the $j\omega$ axis causes a longer transient response.

So far, we have related the mathematical transfer functions of some simple circuits to their associated poles and zeroes in the complex-frequency plane. From these functions we have derived the circuit's frequency response (and hence its Bode

plot), and also its transient response. Because both the integrator and the RC filter have only one s in the denominator of their transfer functions, they each have only one pole. That is, they are first-order filters.

But as we can see from Figure 1b, the first-order filter does not provide a very selective frequency response. To tailor a filter more closely to our needs, we must move on to higher orders. And from now on, we shall describe the transfer function using $f(s)$ rather than the cumbersome V_{OUT}/V_{IN} .

Second Order Lowpass Filters

A second order filter has s^2 in the denominator and two poles in the complex plane. You can obtain such a response by using inductance and capacitance in a passive circuit, or by creating an active circuit of resistors, capacitors and amplifiers. Consider the passive LC filter of Figure 3a, for instance. We can show that its transfer function has the form

$$f(s) = \frac{X_C}{R + X_L + X_C} = \frac{1/sC}{R + sL + 1/sC} = \frac{1}{LCs^2 + RCs + 1}$$

and if we define $\omega_0^2 = 1/LC$ and $Q = \omega_0 L/R$, then

$$f(s) = \frac{\omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2}$$

where ω_0 is the filter's characteristic frequency and Q is the quality factor (lower R means higher Q).

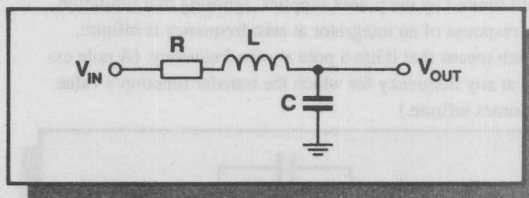


Figure 3a. RLC lowpass filter

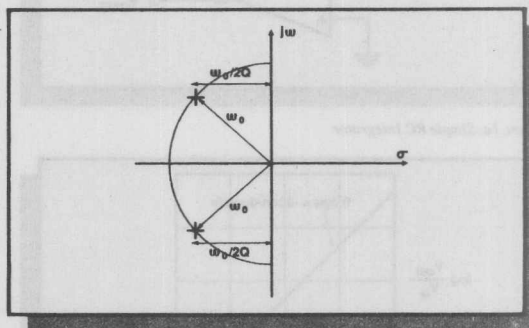


Figure 3b. Pole-Zero diagram of RLC lowpass filter

The poles occur at s values for which the denominator becomes zero. That is, when $s^2 + s\omega_0/Q + \omega_0^2 = 0$. We can solve this equation by remembering that the roots of $ax^2 + bx + c = 0$ are given by

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

In this case $a = 1$, $b = \omega_0/Q$, and $c = \omega_0^2$. The term $(b^2 - 4ac)$ equals $\omega_0^2(1/Q^2 - 4)$, so if Q is less than 0.5 then both roots are real and lie on the negative-real axis. The circuit behaves like two first-order RC filters in cascade. This case isn't very interesting, so we'll consider only the case where $Q > 0.5$ --which means $(b^2 - 4ac)$ is negative and the roots are complex.

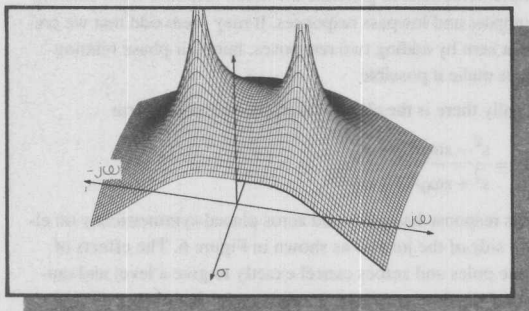


Figure 4a. Complex function of 2nd-order lowpass filter ($Q = 0.707$)

The real part is therefore $-b/2a$, which is $-\omega_0/2Q$, and is common to both roots. The roots' imaginary parts will be equal and opposite in sign. Calculating the position of the roots in the complex plane, we find that they lie at a distance of ω_0 from the origin as shown in Figure 3b. (The associated mathematics, which are straightforward but tedious, will be left as an exercise for the more masochistic readers.)

Varying ω_0 changes the poles' distance from the origin. Decreasing the Q moves the poles towards each other, while increasing the Q moves the poles in a semicircle away from each other and towards the $j\omega$ axis. When $Q = 0.5$ the poles meet at $-\omega_0$ on the negative real axis. In this case the corresponding circuit is equivalent to two cascaded first-order filters, as noted earlier.

Now let's examine the second-order function's frequency response and see how it varies with Q . As before, Figure 4a shows the function as a curved surface, depicted in the three-dimensional space formed by the complex plane and a vertical magnitude vector. $Q = 0.707$, and you can see immediately that the response is a lowpass filter.

The effect of increasing the Q is to move the poles in a circular path towards the $j\omega$ axis. Figure 4b shows the case where $Q = 2$. Because the poles are closer to the $j\omega$ axis they have a greater effect on the frequency response, causing a peak at the high end of the passband.

There is also an effect on the filter's transient response. Because the poles' negative-real part is smaller, an input step function will cause ringing at the filter output. Lower values of Q result in less ringing because the damping is greater. On the other hand, if Q becomes infinite the poles reach the $j\omega$ axis,

causing an infinite frequency response (instability and continuous oscillation) at $\omega = \omega_0$. In the LCR circuit of Figure 3a, this condition would be impossible unless $R = 0$. For filters that contain amplifiers, however, the condition is possible and must be considered in the design process.

A second-order filter provides the variables ω_0 and Q , which allow us to place poles wherever we want in the complex plane. These poles must, however, occur as complex-conjugate pairs,

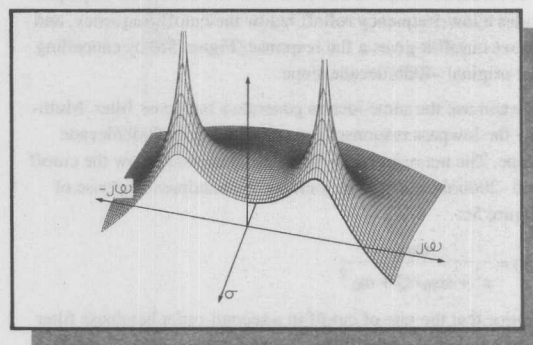


Figure 4b. Complex function of 2nd-order lowpass filter ($Q = 2$)

in which the real parts are equal and the imaginary parts have opposite sign. This flexibility in pole placement is a powerful tool, and one that makes the second-order stage a useful component in many switched-capacitor filters. As in the first-order case, the second-order, lowpass transfer function tends to zero as frequency tends to infinity. The second-order function decreases twice as fast, however, because of the s^2 factor in the denominator. The result is a double zero at infinity.

Having discussed first- and second-order lowpass filters, we now need to extend our ideas in two directions. First, to discuss other filter configurations such as highpass and bandpass sections, and second, to talk about higher-order filters.

Highpass and Bandpass Filters

To change a lowpass filter into a highpass filter we turn the s plane inside out, making low frequencies high and high frequencies low. The double zero at infinite frequency goes to zero frequency, and the finite response at zero frequency becomes infinite. To accomplish this transformation we make $s = \omega_0^2/s$, so that $s \rightarrow \infty$ when $\omega_0^2/s \rightarrow 0$ and vice versa. At ω_0 the old and new values of s are identical. The double zero that was at $s = 1$ moves to zero and the finite response we had at $s = 0$ moves to infinity, producing a highpass filter:

$$f(s) = \frac{\omega_0^2}{\omega_0^4/s^2 + \omega_0^3/Qs + \omega_0^2}$$

If we multiply numerator and denominator by s^2/ω_0^2 ,

$$f(s) = \frac{s^2}{s^2 + s\omega_0/Q + \omega_0^2}$$

This form is the same as before, except the numerator is s^2 instead of ω_0^2 . In other words, we can transform a lowpass function to a highpass one by changing the numerator, leaving the denominator alone.

The Bode plot offers another perspective on lowpass-to-highpass transformations. Figure 5a shows the Bode plot of a second-order lowpass function: flat to the cutoff frequency, then decreasing at -40db/decade. Multiplying by s^2 adds a +40db/decade slope to this function. The additional slope provides a low-frequency rolloff below the cutoff frequency, and above cutoff it gives a flat response (Figure 5b) by cancelling the original -40db/decade slope.

We can use the same idea to generate a bandpass filter. Multiplying the lowpass response by s , which adds a +20db/decade slope. The net response is then +20db/decade below the cutoff and -20db/decade above, yielding the bandpass response of Figure 5c:

$$f(s) = \frac{\omega_0 s}{s^2 + s\omega_0/Q + \omega_0^2}$$

Notice that the rate of cutoff in a second-order bandpass filter is half that of the other types, because the available 40db/decade slope must be shared between the two skirts of the filter.

In summary, second-order lowpass, bandpass and highpass functions in normalized form have the same denominator, but they have numerators of ω_0^2 , $\omega_0 s$ and s^2 respectively.

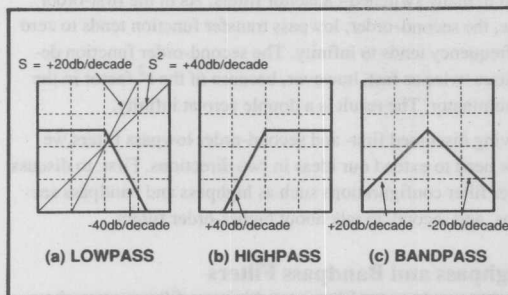


Figure 5. Bode plots of 2nd-order filters

Notch and Allpass Filters

A notch, or bandstop, filter rejects frequencies in a certain band while passing all others. Again, you derive this filter's transfer function by changing the numerator of the standard second-order characteristic:

$$f(s) = \frac{s^2 + \omega_Z^2}{s^2 + s\omega_0/Q + \omega_0^2}$$

Consider the limit cases. When $s = 0$, $f(s)$ reduces to ω_Z^2/ω_0^2 , which is finite. When $s \rightarrow \infty$ the equation reduces to 1. At $s = j\omega_Z$, the numerator becomes zero, $f(s)$ becomes zero (a double zero, in fact, because of s^2 in the numerator), and we have the

characteristic of a notch filter. The gain at frequencies above and below the notch will differ unless $\omega_Z = \omega_0$. The notch filter equation can also be expressed as follows:

$$f(s) = \frac{s^2 + \omega_Z^2}{s^2 + s\omega_0/Q + \omega_0^2} = \frac{s^2}{s^2 + s\omega_0/Q + \omega_0^2} + \frac{\omega_Z^2}{s^2 + s\omega_0/Q + \omega_0^2}$$

In other words, the notch filter is based on the sum of a lowpass and a highpass characteristic. We use this fact in practical filter implementations to generate the notch response from existing highpass and lowpass responses. It may seem odd that we create a zero by adding two responses, but their phase relationships make it possible.

Finally there is the allpass filter, which has the form

$$f(s) = \frac{s^2 - s\omega_0/Q + \omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2}$$

This response has poles and zeros placed symmetrically on either side of the $j\omega$ axis as shown in Figure 6. The effects of these poles and zeroes cancel exactly to give a level and uniform frequency response. It might seem that a piece of wire could provide this effect more cheaply, but unlike a wire, the allpass filter provides a useful variation of phase response with frequency.

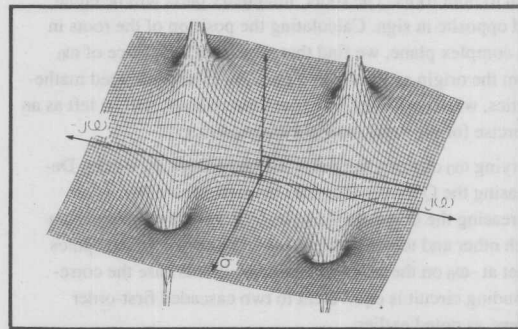


Figure 6. Complex function of 2nd-order allpass filter

We have now covered first- and second-order filters with lowpass, highpass, bandpass, notch and allpass configurations. The MF10 and MAX260 series of switched-capacitor IC filters use these same techniques, cascading first- and second-order sections to construct filters of any order. Let us see how this is done.

Higher Order Filters

We are fortunate in not having to treat the higher-order filters separately, because a polynomial in s of any length can be factored into a series of quadratic terms (plus a single first-order term, if the polynomial is odd). A fifth-order lowpass filter, for instance, might have the transfer function

$$f(s) = \frac{1}{s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0}$$

where all the a_n are constants. We can factor the denominator as follows:

$$f(s) = \frac{1}{(s^2 + s\omega_1/Q_1 + \omega_1^2)(s^2 + s\omega_2/Q_2 + \omega_2^2)(s + \omega_3)}$$

which is the same as

$$f(s) = \frac{1}{(s^2 + s\omega_1/Q_1 + \omega_1^2)} \times \frac{1}{(s^2 + 3\omega_2/Q_2 + \omega_2^2)} \times \frac{1}{(s + \omega_3)}$$

The last equation represents a filter that we can physically realise as two second-order sections and one first-order section, all in cascade. This configuration simplifies the design by making it easier to visualize the response in terms of poles and zeroes in the complex-frequency plane. We know that each second-order term contributes one complex-conjugate pole pair, and that the first-order term contributes one pole on the negative-real axis. If the transfer function has a higher-order polynomial in the numerator, that polynomial can be factored as well, which means that the second-order sections will be something other than lowpass sections.

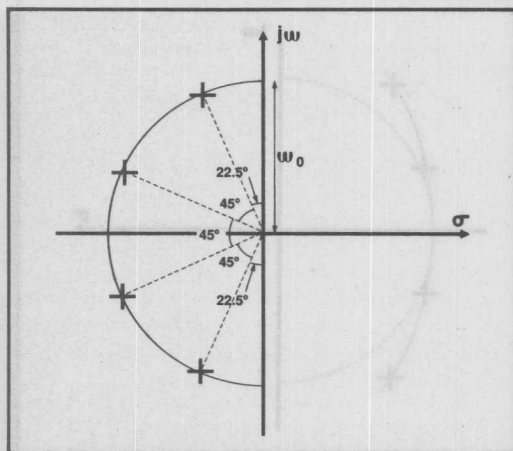


Figure 7a. Pole-Zero diagram of 4th-order Butterworth lowpass filter

Using the synthesis principles described above, we can build a great variety of filters simply by placing poles and zeroes at different positions in the complex-frequency plane. Most applications require only a restricted number of these possibilities, however. And for these, many earlier experimenters such as Butterworth and Chebychev have already worked out the details.

The Butterworth Filter

A type of filter that is common to many applications requires a response that is flat in the passband but cuts off as sharply as possible thereafter. You can obtain that response by arranging the poles of a lowpass filter with equal spacing around a semi-circular locus, and the result will be a Butterworth filter. The

pole-zero diagram of Figure 7a, for example, represents a fourth-order type of Butterworth filter.

The poles in Figure 7a have different Q values, but they all have the same ω_0 because they are all the same distance from the origin. The three-dimensional surface corresponding to this filter (Figure 7b) illustrates how, as the effect of the lowest- Q pole starts to wear off, the next pole takes over, and the next, until you run out of poles and the response falls off at -80db/decade.

You can build Butterworth versions of highpass, bandpass, and other filter types, but the poles of these filters will not be arranged in a simple semicircle. In most cases you begin by designing a lowpass filter, then applying transformations to generate the other types (such as the $s \rightarrow 1/s$ that we used earlier to change a lowpass into a highpass).

The Chebychev Filter

By bringing poles closer to the $j\omega$ axis (increasing their Q s) we can make a filter whose frequency cutoff is steeper than a Butterworth. This arrangement has a penalty--the effects of each pole will be visible in the filter response, giving a variation in amplitude known as ripple in the passband. With proper pole arrangement the variations can be made equal, however, which results in a Chebychev filter.

You derive a Chebychev filter from a Butterworth by moving each pole closer to the $j\omega$ axis in the same proportion, so that the poles lie on an ellipse (Figure 8a). Figure 8b demonstrates how each pole contributes one peak to the passband ripple. Moving the poles closer to the $j\omega$ axis increases the passband ripple, but provides a more abrupt cutoff in the stopband. The Chebychev filter therefore offers a tradeoff between ripple and cutoff. In this respect the Butterworth filter in which passband ripple has been set to zero, is a special case of the Chebychev.

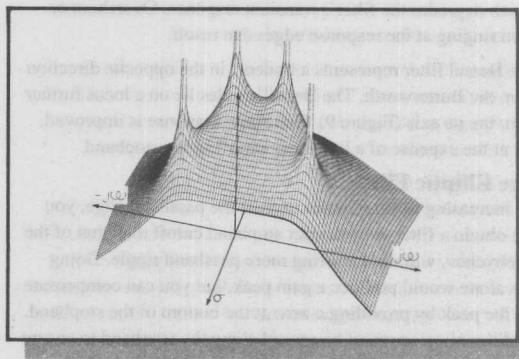


Figure 7b. Complex function of 4th-order Butterworth lowpass filter

The Bessel Filter

Butterworth and Chebychev filters with sharp cutoffs carry a penalty that is evident from the positions of their poles in the s plane. Bringing the poles closer to the $j\omega$ axis increases their Q ,

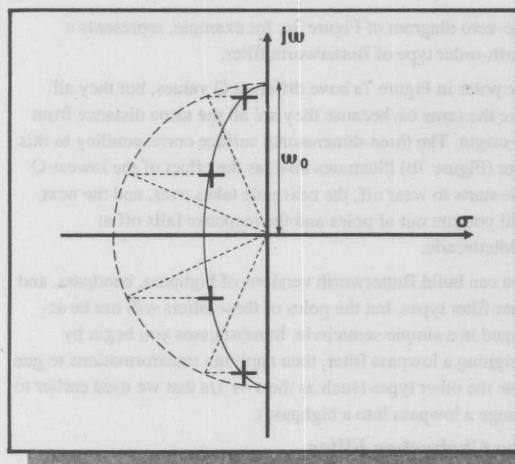


Figure 8a. Pole-Zero diagram of 4th-order Chebychev lowpass filter

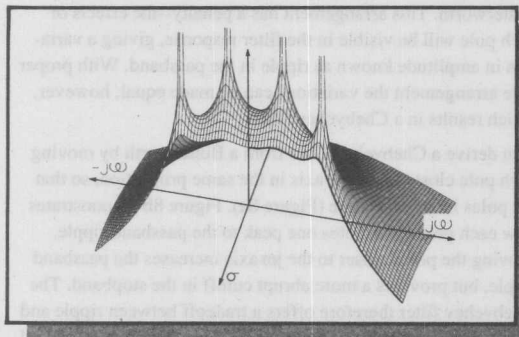


Figure 8b. Complex function of 4th-order Chebychev lowpass filter

which degrades the filter's transient response. Overshoot or even ringing at the response edges can result.

The Bessel filter represents a tradeoff in the opposite direction from the Butterworth. The Bessel's poles lie on a locus further from the $j\omega$ axis (Figure 9). Transient response is improved, but at the expense of a less-steep cutoff in the stopband.

The Elliptic Filter

By increasing the Q of poles nearest the passband edge, you can obtain a filter with sharper stopband cutoff than that of the Chebychev, without incurring more passband ripple. Doing this alone would produce a gain peak, but you can compensate for the peak by providing a zero at the bottom of the stopband. Additional zeroes must be spaced along the stopband to ensure that the filter response remains below the desired level of stopband attenuation. Figure 10a shows the pole-zero diagram for this type--an elliptic filter. Figure 10b shows the corresponding transfer-function surface. As you may imagine, the elliptic filter's high- Q poles produce a transient response that is even worse than that of the Chebychev.

Note that all the filters described have the same number of zeros as poles (this must be the case, or the transfer function would not be a dimensionless expression). Elliptic filters, for example, space their zeroes along the $j\omega$ axis in the stopband. In the case of Bessel, Butterworth, and Chebychev all the zeros are on top of each other at infinity. Because there are no zeros explicit in the numerator, these filter types are sometimes called all-pole filters.

We have now extended our ideas to cover not only first- and second-order filters, but also filters of higher order, including some particularly useful cases. Now it's time to get away from abstract theory and talk about practical circuits.

The State Variable Filter

As demonstrated earlier, we can construct any filter from first- and second-order building blocks. You can regard the first-order filter as a special case of the second order, so our basic building block should be a second-order section, from which we can derive lowpass, highpass, bandpass, notch, or allpass characteristics.

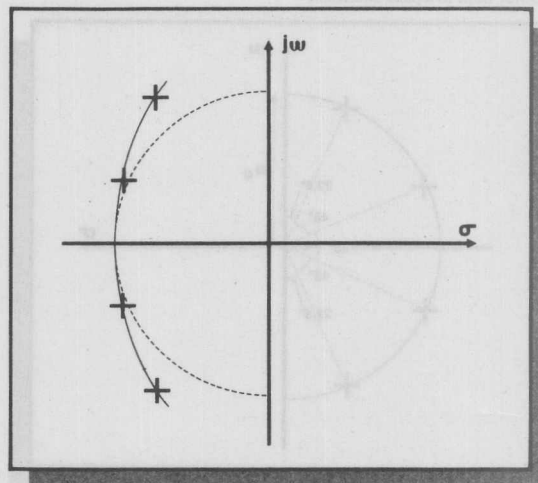


Figure 9. Pole-Zero diagram of 4th-order Bessel lowpass filter

The state variable filter is a convenient realization for the second-order section. It uses two cascaded integrators and a summing junction as shown in Figure 11. We know that the characteristic of an integrator is simply ω_0/s , but to demonstrate the principle while simplifying the mathematics, we can assume that both integrators have $\omega_0 = 1$, and that their characteristic is simply $1/s$. Then we can write equations for each of the integrators in Figure 11:

$$L = B/s \quad \text{or} \quad B = sL$$

$$B = H/s \quad \text{or} \quad H = sB = s^2L$$

The equation for the summing junction in Figure 11 is simply $H = I - B - L$.

If we substitute for H and B using the integrator equations, we get:

$$s^2 L = I - sL - L$$

or

$$s^2 L + sL + L = I,$$

whence

$$L(s^2 + s + 1) = I,$$

or

$$\frac{L}{I} = \frac{1}{s^2 + s + 1}$$

which is the classic normalized lowpass response. Because $B = sL$ and $H = s^2 L$,

$$\frac{B}{I} = \frac{s}{s^2 + s + 1} \quad \text{and} \quad \frac{H}{I} = \frac{s^2}{s^2 + s + 1}$$

These are, respectively, the classic bandpass and highpass responses.

Thus one filter provides simultaneous lowpass, bandpass, and highpass outputs. We can create actual filters with real values of ω_0 and Q from these equations by building integrators with $\omega_0 \neq 1$, and feedback factors to the summing junction with values $\neq 1$.

In theory you can create higher-order filters by cascading more than two integrators. Some integrated-circuit filters use this approach, but it has drawbacks. To program these filters you must calculate coefficient values for the higher-order polynomial. Also, a long string of integrators introduces stability

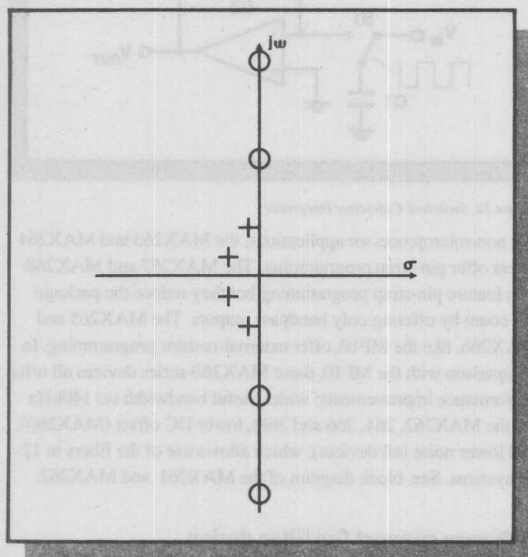


Figure 10a. Pole-Zero diagram of 4th-order Elliptic lowpass filter

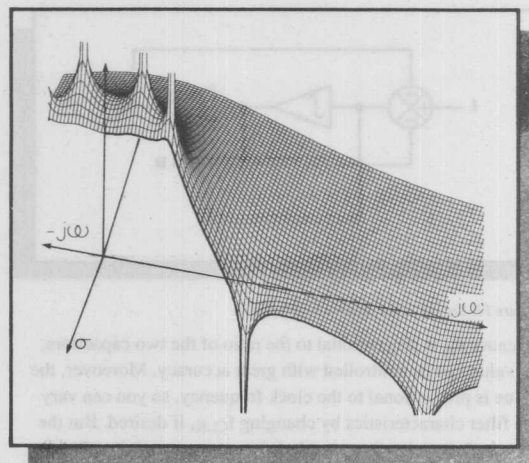


Figure 10b. Complex function of 4th-order Elliptic lowpass filter

problems. By limiting ourselves to second-order sections, we have the advantage of working directly with the ω_0 and Q variables associated with each pole.

Switched-Capacitor Filters

The characteristics of all active filters, regardless of architecture, depend on the accuracy of their RC time constants.

Because the typical precision achieved for integrated resistors and capacitors is about $\pm 30\%$, a designer is handicapped when attempting to use absolute values for the components in an integrated filter circuit. The ratio of capacitor values on a chip can be accurately controlled, however, to about one part in 2000. Switched-capacitor filters use these capacitor ratios to achieve precision without the need for precise external components.

In the switched-capacitor integrator of Figure 12, the combination of C_1 and the switch simulates a resistor. The switch S_1 toggles continuously at a clock frequency f_{CLK} . Capacitor C_1 charges to V_{IN} when S_1 is to the left. When it switches to the right, C_1 dumps charge into the integrator's summing node, from which it flows into the capacitor C_2 . The charge on C_1 during each clock cycle is

$$Q = C_1 V_{IN},$$

and therefore the average current transferred to the summing junction is

$$I = Qf_C = C_1 V_{IN} \cdot f_C.$$

Notice that the current is proportional to V_{IN} , so we have the same effect as a resistor of value

$$R = \frac{V_{IN}}{I} = \frac{1}{C_1 f_C}$$

The integrator's ω_0 is therefore

$$\omega_0 = \frac{1}{RC_2} = \frac{C_1 f_C}{C_2}$$

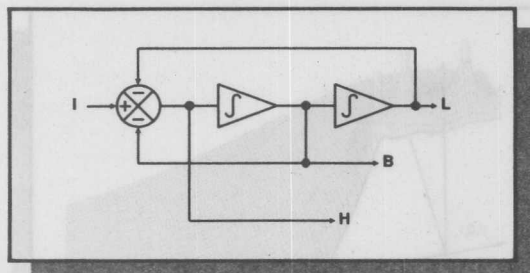


Figure 11. Second-order, state-variable filter

Because ω_0 is proportional to the ratio of the two capacitors, its value can be controlled with great accuracy. Moreover, the value is proportional to the clock frequency, so you can vary the filter characteristics by changing f_{CLK} , if desired. But the switched capacitor is a sampled-data system, and therefore is not completely equivalent to the time-continuous RC integrator. The differences, in fact, pose three issues for a designer.

First, the signal passing through a switched capacitor is modulated by the clock frequency. If the input signal contains frequencies near the clock frequency, they can intermodulate and cause spurious output frequencies within the system bandwidth. For many applications this is not a problem because the input bandwidth has already been limited to less than half the clock frequency. If not, the switched-capacitor filter must be preceded by an anti-aliasing filter that removes any components of input frequency above one half of the clock frequency.

Second, the integrator output (Figure 12) is not a linear ramp, but a series of steps at the clock frequency. There may be small spikes at the step transitions caused by charge injected by the switches. These aberrations may not be a problem if the system bandwidth following the filter is much lower than the clock frequency. Otherwise, you must again add another filter at the output of the switched-capacitor filter to remove the clock ripple.

Third, the behaviour of the switched-capacitor filter differs from the ideal, time-continuous model because the input signal is sampled only once per clock cycle. The filter output deviates from the ideal as the filter's pole frequency approaches the clock frequency, particularly for low values of Q . You can, however, calculate these effects and allow for them during the design process. Maxim's filter-design software, for instance, performs these corrections.

Considering the above, it is best to keep the ratio of clock-to-center frequency as large as possible. Typical ratios for switched-capacitor filters range from about 28:1 to 200:1. The MAX262, for example, allows a maximum clock frequency of 4MHz, so using the minimum ratio of 28:1 gives a maximum center frequency of 140kHz. At the low end, switched-capacitor filters have the advantage that they can handle low

frequencies without using uncomfortably large values of R and C . You simply lower the clock frequency.

Some Real Devices

The second-order, state-variable filter, built with switched-capacitor techniques, is the primary component in programmable filter chips such as the MF10, as well as the more recent series from Maxim: the MAX260 to MAX268. Each of these IC devices contain two second-order, state-variable filter sections, which lets you configure a single chip as a first-, second-, third-, or fourth-order filter. For higher-order filters, you use two or more chips.

The MF10 adds sophistication to the state-variable filter by incorporating both a summing amplifier and a summing node at the input. These extra feedback connections let you configure the chip's first output as highpass, notch, or allpass, while the other two outputs remain bandpass and lowpass as specified. You set the center frequency and Q for each section by adding external resistors in the appropriate ratios. The MF10 has become an industry standard over the years, particularly for the telephone-grade audio found in telecommunication systems, where the chip's upper-frequency limit of 30kHz is not a problem.

More recently, Maxim has introduced an improved series of filters based on the same state-variable architecture. The series MAX260 to 262, for instance, consists of chips that are programmed directly from a microprocessor bus. These products, which eliminate external programming resistors, can easily implement adaptive or frequency-agile filters.

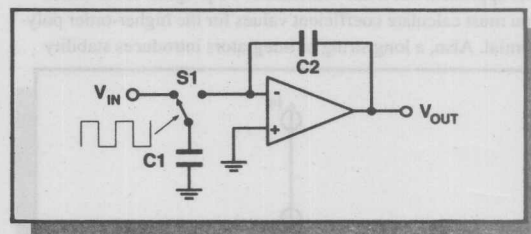


Figure 12. Switched-Capacitor Integrator

For non-microprocessor applications, the MAX263 and MAX264 filters offer pin-strap programming. The MAX267 and MAX268 also feature pin-strap programming but they reduce the package pin count by offering only bandpass outputs. The MAX265 and MAX266, like the MF10, offer external-resistor programming. In comparison with the MF10, these MAX260-series devices all offer performance improvements: wider useful bandwidth (to 140kHz for the MAX262, 264, 266 and 268), lower DC offset (MAX260), and lower noise (all devices), which allows use of the filters in 12-bit systems. See block diagram of the MAX261 and MAX262.

Software support for filter design

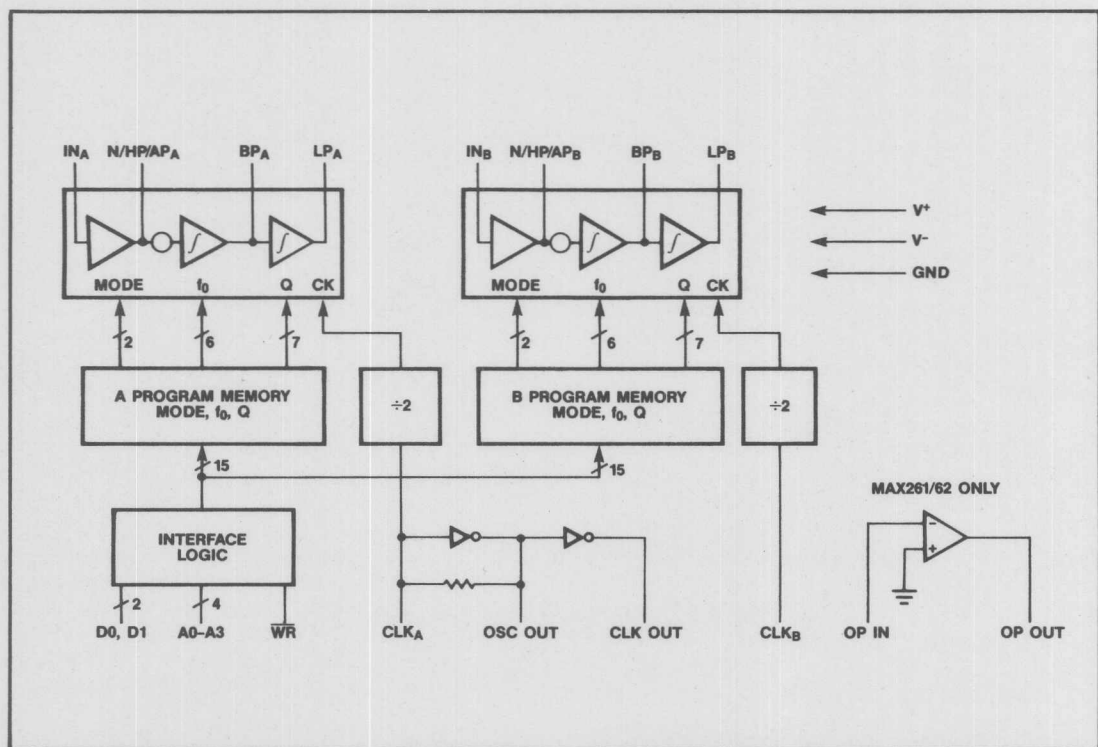
As companion to the MAX260 series of devices, Maxim has introduced a software-design package that runs on industry-stan-

ard PCs. By answering a series of prompts, the user specifies the type of filter required (lowpass, bandpass, etc), the desired polynomial (Butterworth, Chebychev or Elliptic), and the passband and stopband characteristics in terms of frequency and attenuation. The software then automates the design process by calculating the necessary filter order, along with the required frequency and Q for all poles and zeroes.

The system then passes this information to other software modules for calculation of the physical-filter parameters (digital-programming coefficients are appropriate for the MAX260-264 and for the MAX267 and 268, or resistor values for the MF10, MAX265 and MAX266). You can calculate and display the filter characteristic in graphic form. Then, by introducing tolerances you can allow for worst-case component variations. This software is available for \$2.00 to designers working with products of the MAX260 series.

Conclusion

The purpose of this article was to introduce the concepts and terminology associated with switched-capacitor active filters. If you have read and understood the material you should now be able to understand most filter data sheets. A more detailed description of the filter devices and their accompanying software is planned for a later issue.



MAX260/61/62 Block Diagram

